

Features

- Frequency: DC-6GHz
- Small Signal Gain: 21dB Typical
- Gain Flatness: ± 0.3 dB Typical
- Noise Figure: 1.0dB Typical
- P1dB: +28 dBm @VD=+10V
- Psat: +29 dBm @VD=+10V
- Supply voltage:
 - VD = +5V/+8V/+10V@125mA
 - VG = -0.8V to -0.2V
- Input/Output: 50 Ω
- Package Size : 3 x 3x 0.7mm

Typical Applications

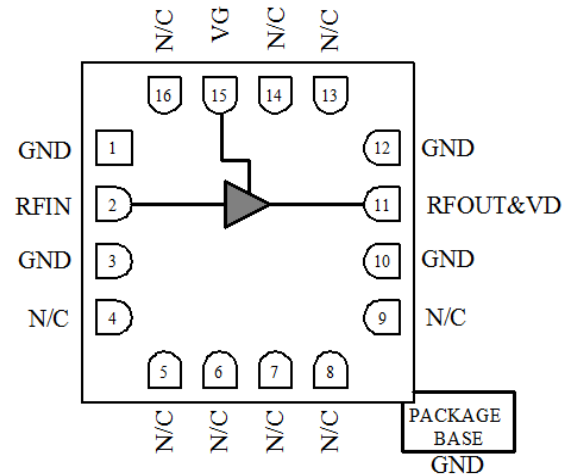
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Electrical Specifications

TA = +25°C, VD= +5V/+8V/10V, VG=-0.8 to -0.2V, IDD = 125mA* Typical

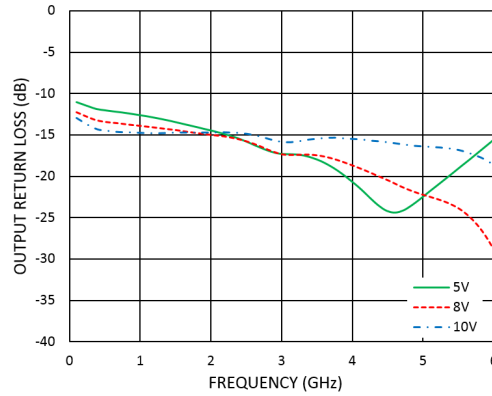
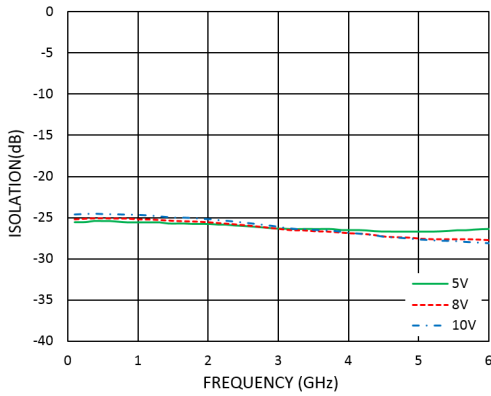
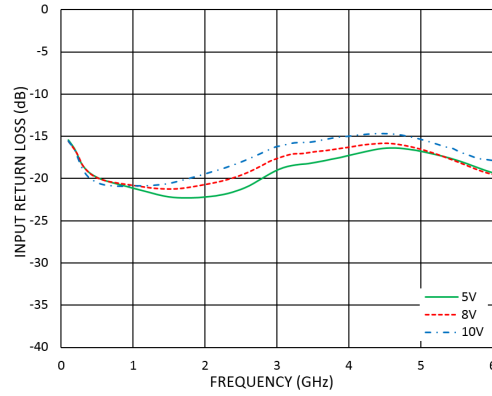
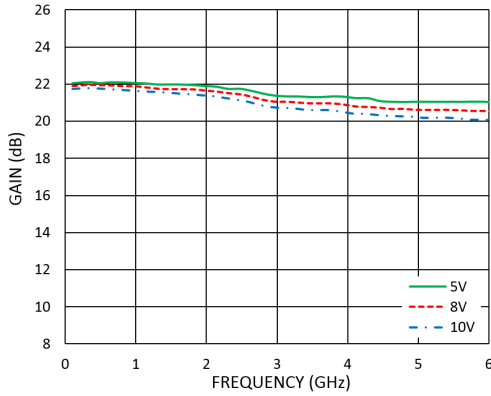
Parameters	VD=+5V			VD=+8V			VD=+10V			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	DC-6			DC-6			DC-6			GHz
Small Signal Gain	20	21		19.5	20.5		19	20		dB
Gain Flatness	± 0.5			± 0.5			± 0.75			dB
Noise Figure	1.1			1.2			1.3			dB
P1dB - Output 1dB Compression	20	22.5		25	26.5		26	28		dBm
Psat - Saturated Output Power	23.5			27.5			29			dBm
OIP3 - Output Third Order Intercept	35			39			40.5			dBm
Input Return Loss	-17			-16			-15			dB
Output Return Loss	-13			-14			-15			dB

*The operating current can be controlled around 125mA by adjusting the VG voltage, and the VG regulation range: -0.8V ~-0.2V.

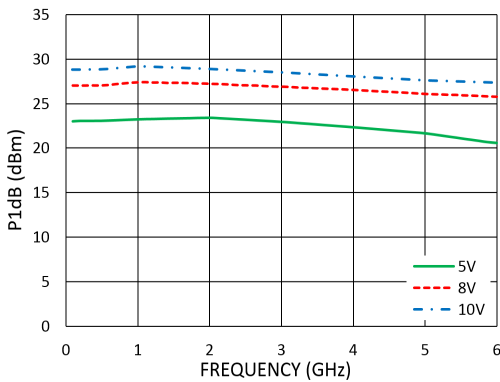
Functional Block Diagram




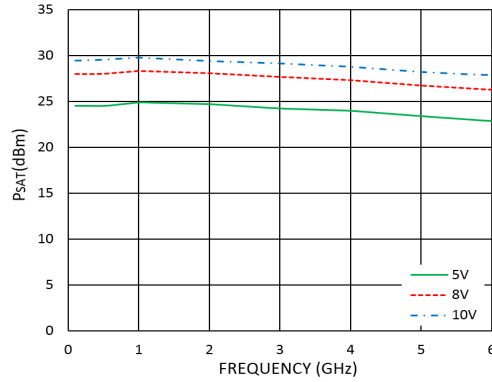
Measurement Plots: S-parameters

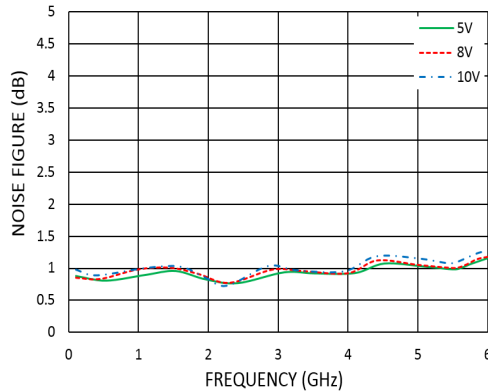


Measurement Plots: P1dB



Measurement Plots: Psat



Measurement Plots: Noise Figure

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+12V
Gate Bias Voltages(VG)	-3V
RF Input Power (RFIN)(VD=+10V)	+20 dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 17.8mW/°C above 85 °C)	1.6W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

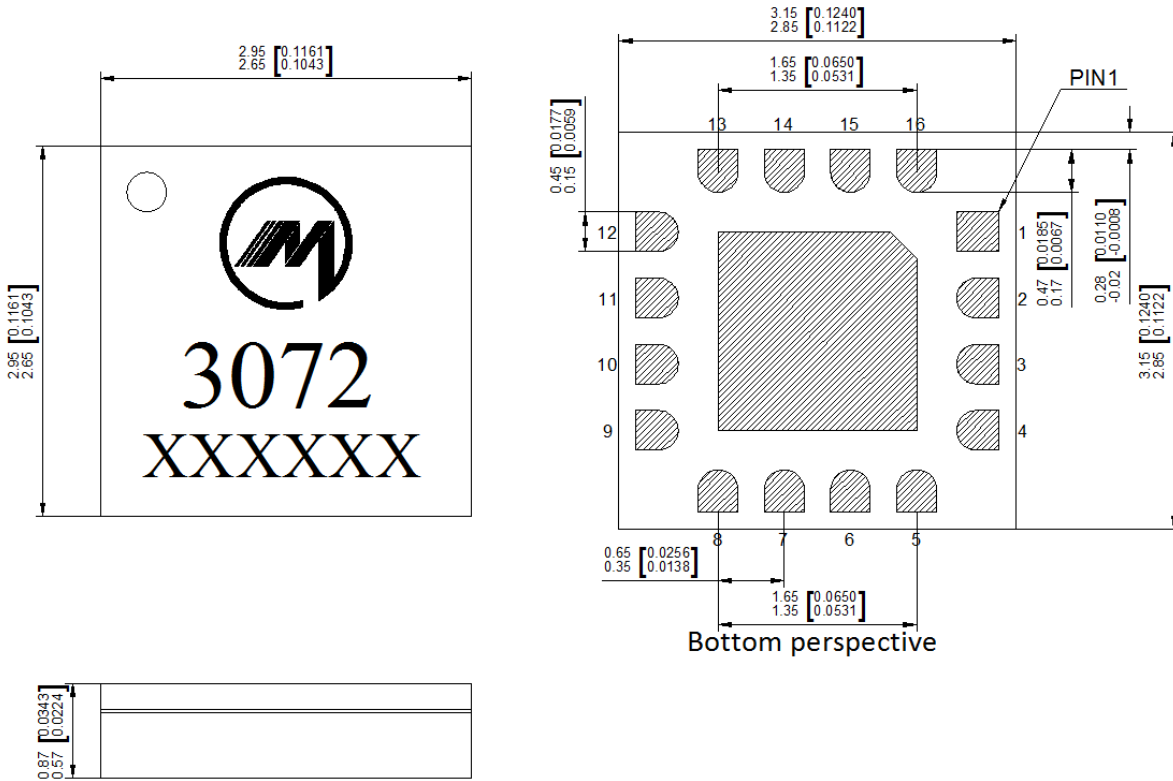
VG (V)	VD (V)	IDD (mA)
-0.8 to -0.2	+5/+8/+10	125



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing: All Dimensions in mm[inches]

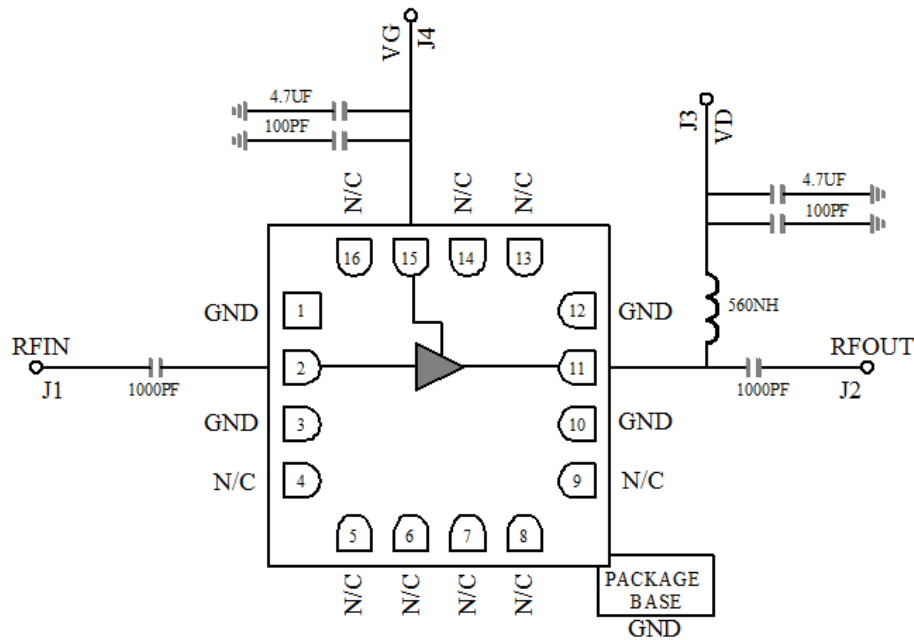


Notes:

1. Package body material : Alumina.
2. Lead and ground paddle plating: Gold flash over nickel.
3. Dimensions are in millimeters(inches).
4. Lead spacing tolerance is non-cumulative.



Assembly Drawing

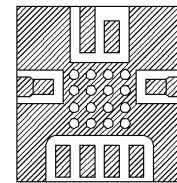
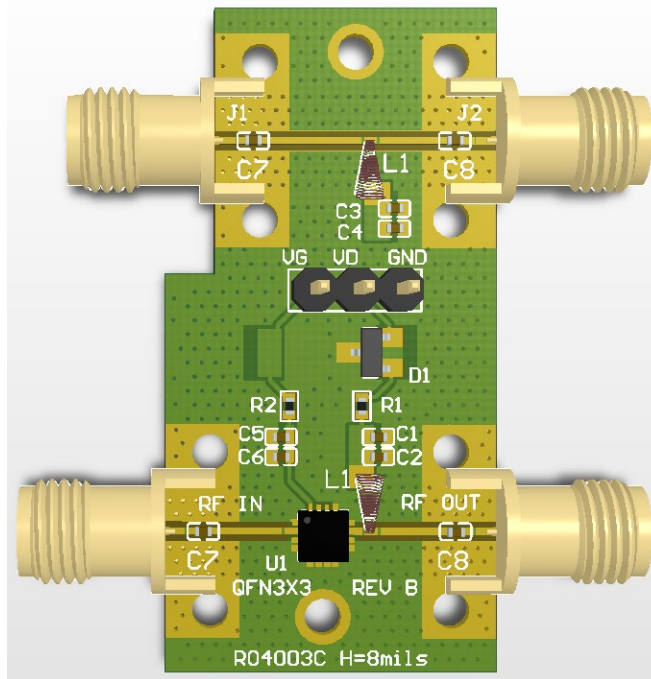


Pin Descriptions

No	Function	Description
4,5,6,7,8,9,13,14,16	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
2	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
11	RF OUT & VD	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
15	VG	Connect to external 100pf and 4.7uf bypass capacitors.
1,3,10,12	GND	These pins & exposed ground paddle must be connected to RF/DC ground
17	GND	Package bottom must be connected to RF/DC ground



Evaluation Board Layout Assembly and Mounting Pattern



Mounting Detail

Top dielectric material is ROGERS 4003C, 0.008 inch thickness with 0.5 oz copper.

The pad pattern shown above has been developed and tested for optimized assembly at Miller. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008~0.01 in. diameter drill, filled with copper plating.

Bill of Materials

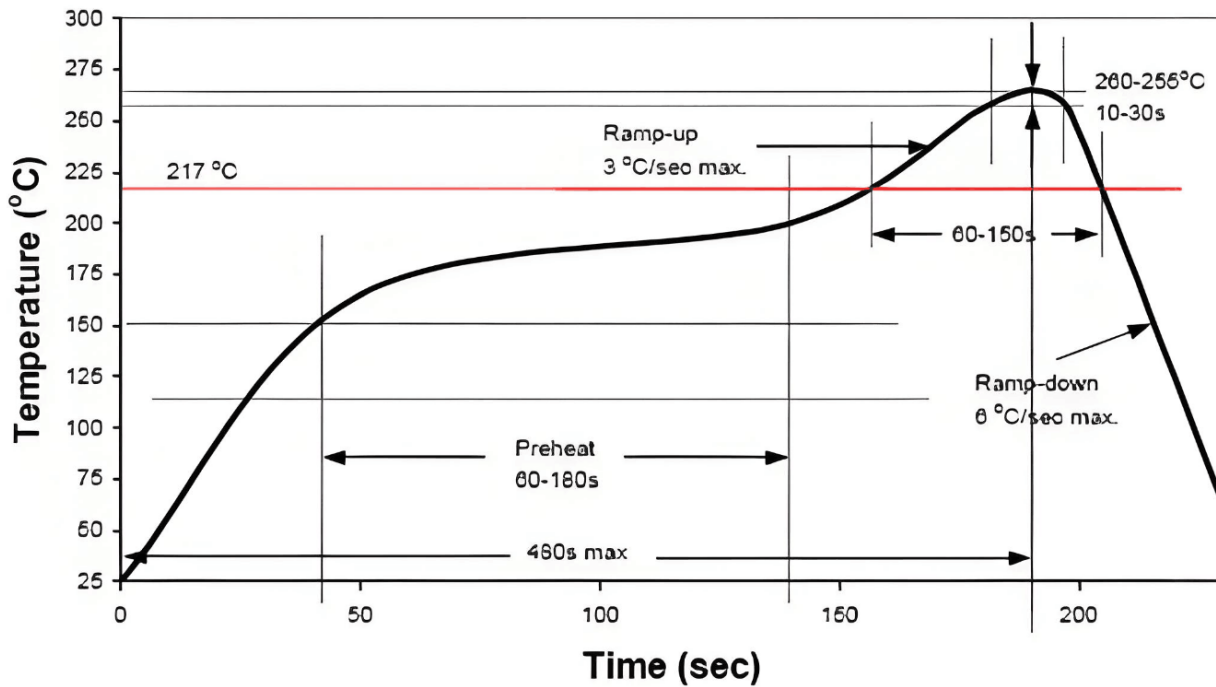
Reference Des.	Value	Description	Manuf.
C1,C5	4.7uF	Cap, 0603, +10V, ±10 %, X5R	Various
C2,C6	100pF	Cap, 0603, +50V, ±5%, X7R	Various
C7,C8	1000pF	Cap, 0402, +50V, ±10%, X7R	Various
R1,R2	0.01 Ω	Res, 0603,0.1W	Various
D1	6.8V	Diode,SOT23,ESD	Various
L1	560nH	Conical Inductor,200mA	Various

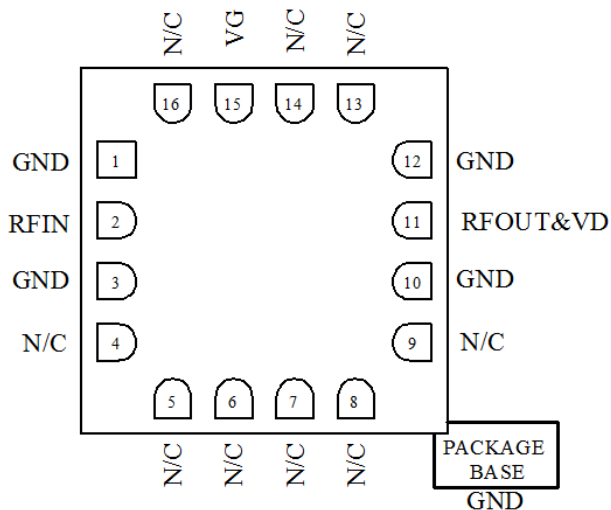


Solderability

1. Compatible with lead-free soldering process with 260°C peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing.
The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile





Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set all the gate bias voltages, VG to $-3V$.
3. Set the drain bias voltages VD to $+5V/+8V/+10V$.
4. Increase the gate bias voltages to achieve a quiescent supply current of 125 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to $-3V$ to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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