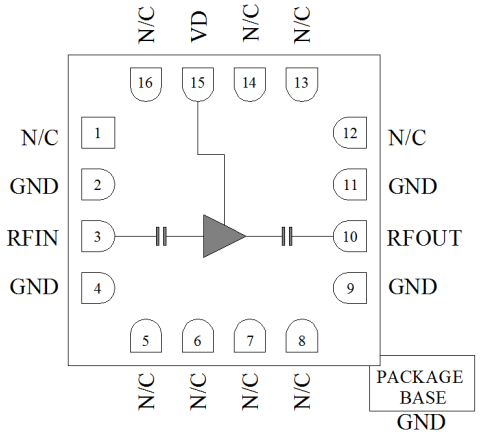
Features

- Single Biasing Voltage (Self Biased)
- Frequency: 0.1-4.5GHz
- Small Signal Gain: 31dB Typical
- Gain Flatness: ±0.5dB Typical
- Noise Figure:0.7dB Typical
- P1dB: 19dBm Typical
- Power Supply: +5V@125mA
- Input/Output: 50Ω
- Package Size : 3 x 3 x 0.7mm

Functional Block Diagram



Typical Applications

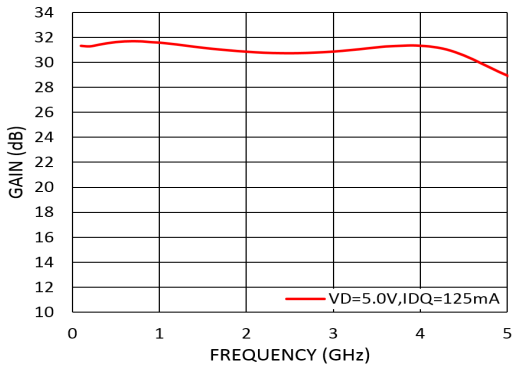
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

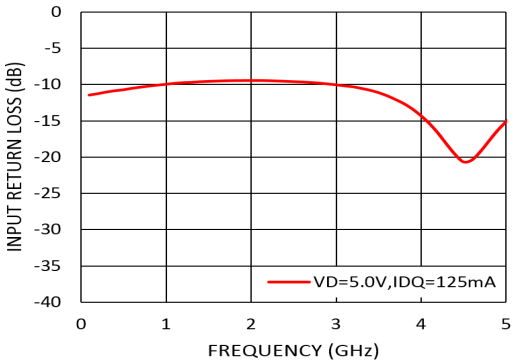
Electrical Specifications

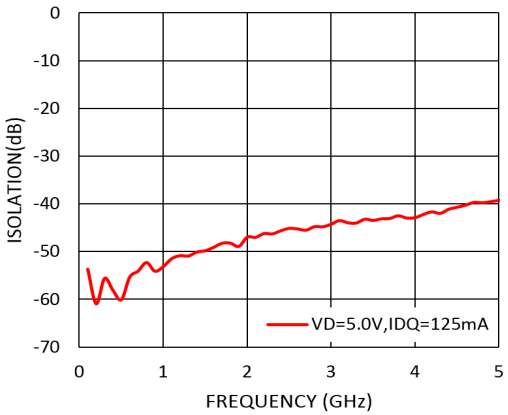
TA = +25°C, VD = +5V, IDD = 125mA Typical

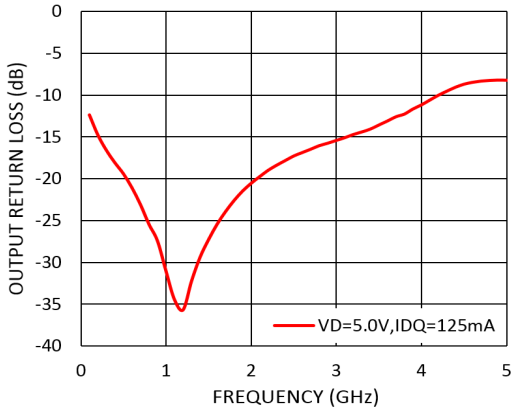
Parameters	Min.	Typ.	Max.	Units
Frequency	0.1		4.5	GHz
Small Signal Gain	30	31		dB
Gain Flatness		±0.5		dB
Noise Figure		0.7		dB
P1dB - Output 1dB Compression	18	19		dBm
Psat - Saturated Output Power		21		dBm
OIP3 - Output Third Order Intercept		29		dBm
Input Return Loss		-10		dB
Output Return Loss		-13		dB

Measurement Plots: S-parameters

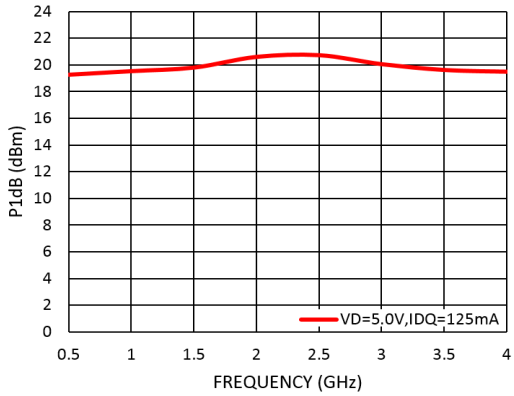




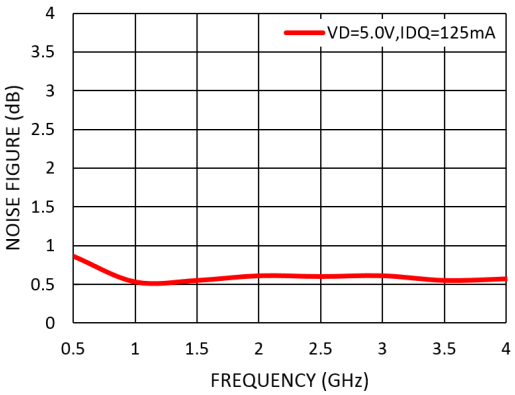




Measurement Plots: P1dB



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+7V
RF Input Power (RFIN)	+18dBm
Channel Temperature	165°C
Continuous Pdiss (T = 85 °C) (derate 10.6mW/°C above 85 °C)	0.95W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

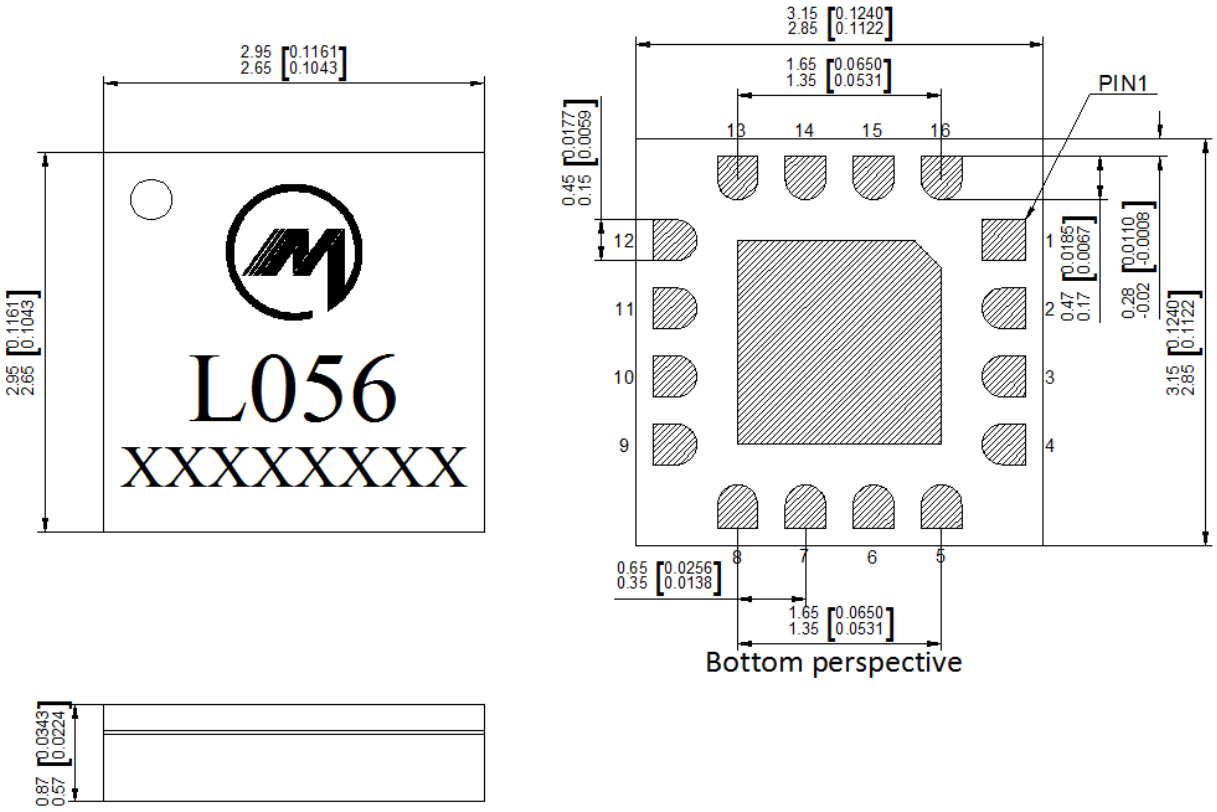
Typical Supply Current vs. VD

VD (V)	IDD (mA)
+5	125

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:

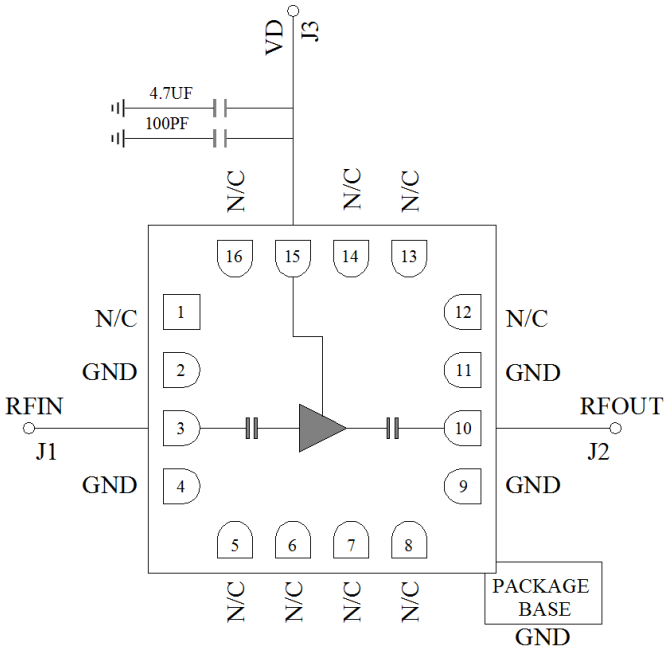
All Dimensions in mm[inches]



Notes:

1. Package body material : Alumina.
2. Lead and ground paddle plating: Gold flash over nickel.
3. Dimensions are in millimeters(inches).
4. Lead spacing tolerance is non-cumulative.

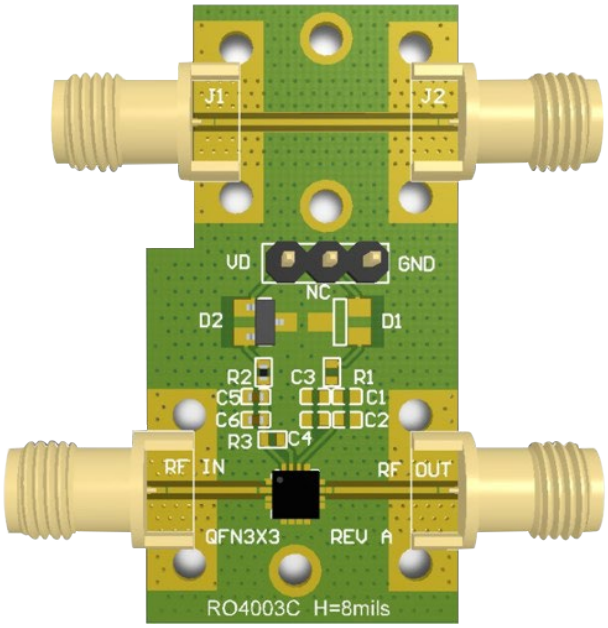
Assembly Drawing

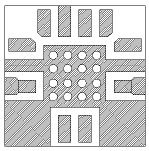


Pin Descriptions

No	Function	Description
1,5,6,7,8,12,13,14,16	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
3	RF IN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
10	RF OUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
15	VD	Connect to external 100pF and 4.7uF bypass capacitors.
2,4,9,11	GND	These pins & exposed ground paddle must be connected to RF/DC ground
17	GND	Package bottom must be connected to RF/DC ground

Evaluation Board Layout Assembly and Mounting Pattern





Mounting Detail

Top dielectric material is ROGERS 4003C, 0.008 inch thickness with 0.5 oz copper.

The pad pattern shown above has been developed and tested for optimized assembly at Miller. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008~0.01 in. diameter drill, filled with copper plating.

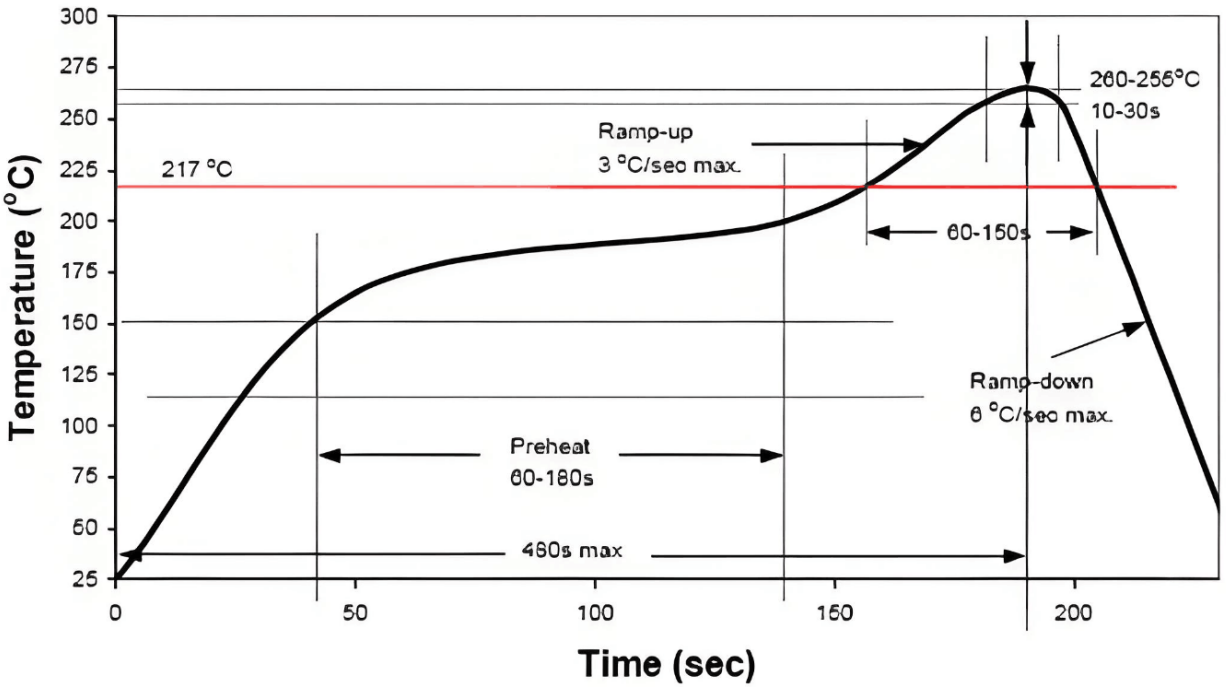
Bill of Materials

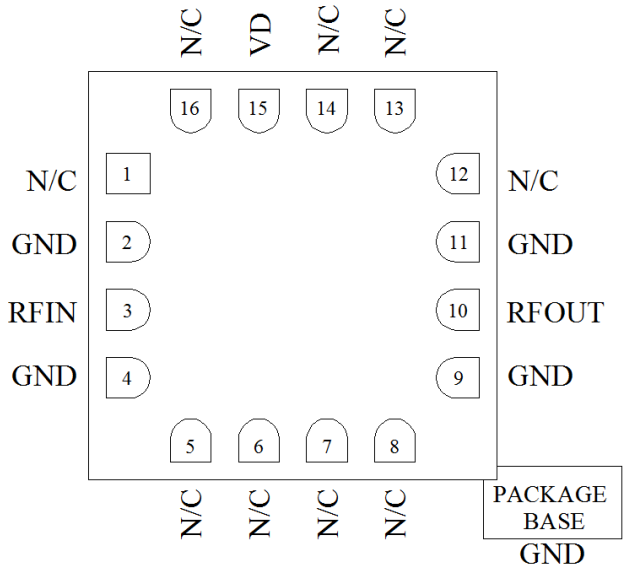
Reference Des.	Value	Description	Manuf.
C5	4.7uF	Cap, 0603, +10V, ±10 %, X5R	Various
C6	100pF	Cap, 0603, +50V, ±5%, X7R	Various
R2	0.01 Ω	Res, 0603,0.1W	Various
D2	6.8V	Diode,SOT23,ESD	Various
C1,C2,C3,C4,R1,R3,D1	/	/	/

Solderability

1. Compatible with lead-free soldering process with 260℃ peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile





Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Apply positive drain voltage VD and set to +5.0 V .
3. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Turn off the positive drain voltage VD.