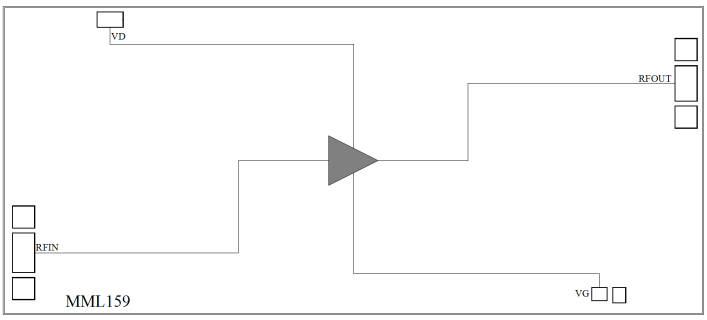
Features

- Frequency: DC-20GHz
- Small Signal Gain: 18dBTypical
- Gain Flatness: ±1.0dB Typical
- Noise Figure:2.0dB Typical
- P1dB: 19dBm Typical
- Power Supply:
  VD=+8V@110mA ,VG=-0.36V
- Input/Output: 50Ω
- Chip Size: 3.1 x 1.36 x 0.1mm

Functional Block Diagram



Typical Applications

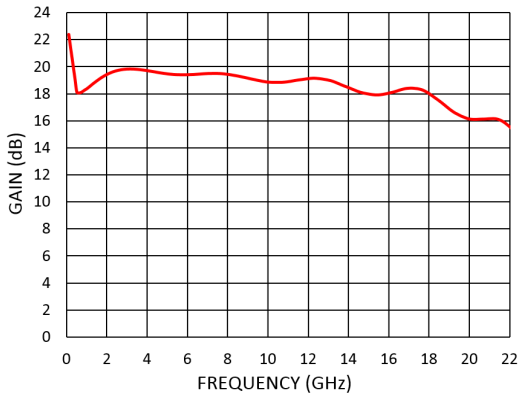
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

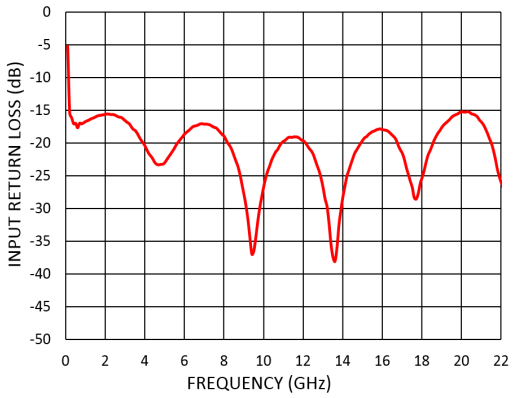
Electrical Specifications

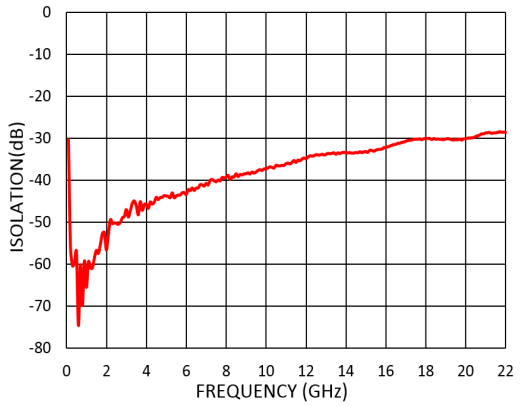
TA = +25°C, VD = +8V , VG=-0.36V , IDD = 110mA Typical

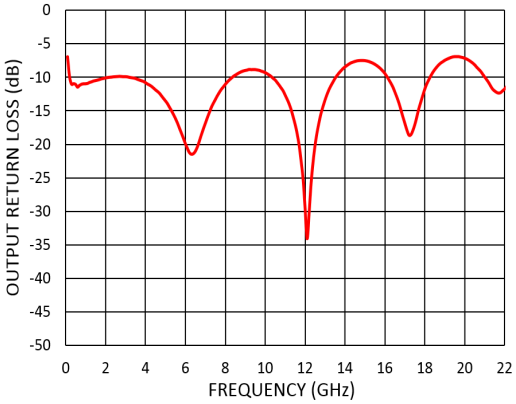
Parameters	Min.	Typ.	Max.	Units
Frequency	DC		20	GHz
Small Signal Gain	15.5	18		dB
Gain Flatness		±1.0		dB
Noise Figure		2.0		dB
P1dB - Output 1dB Compression	15	19		dBm
Psat - Saturated Output Power		20		dBm
OIP3 - Output Third Order Intercept		30		dBm
Input Return Loss		-17		dB
Output Return Loss		-10		dB

Measurement Plots: S-parameters

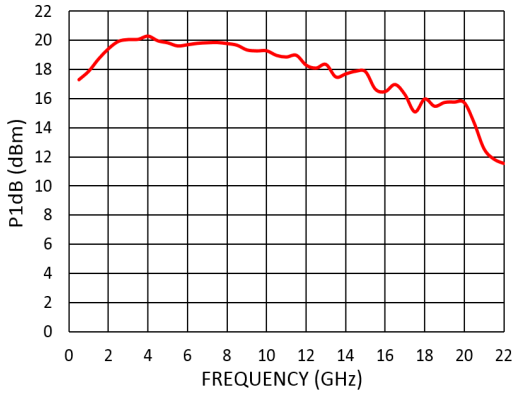




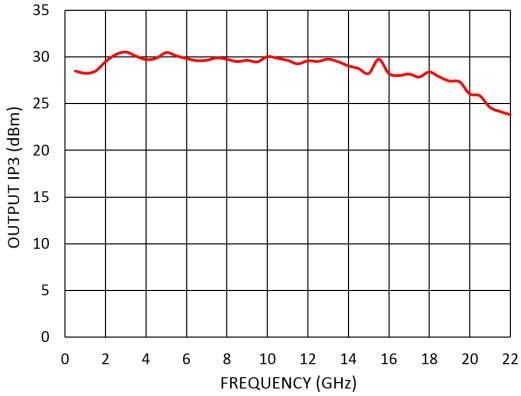




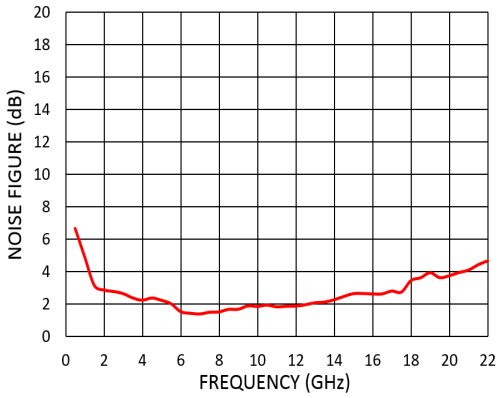
Measurement Plots: P1dB



Measurement Plots: OIP3



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+9V
Gate Bias Voltage (VG)	0 to -3V
RF Input Power (RFIN)	+23dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 12.2mW/°C above 85 °C)	1.1W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +125 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

VD (V)	VG (V)	IDD (mA)
+8	-0.36	110

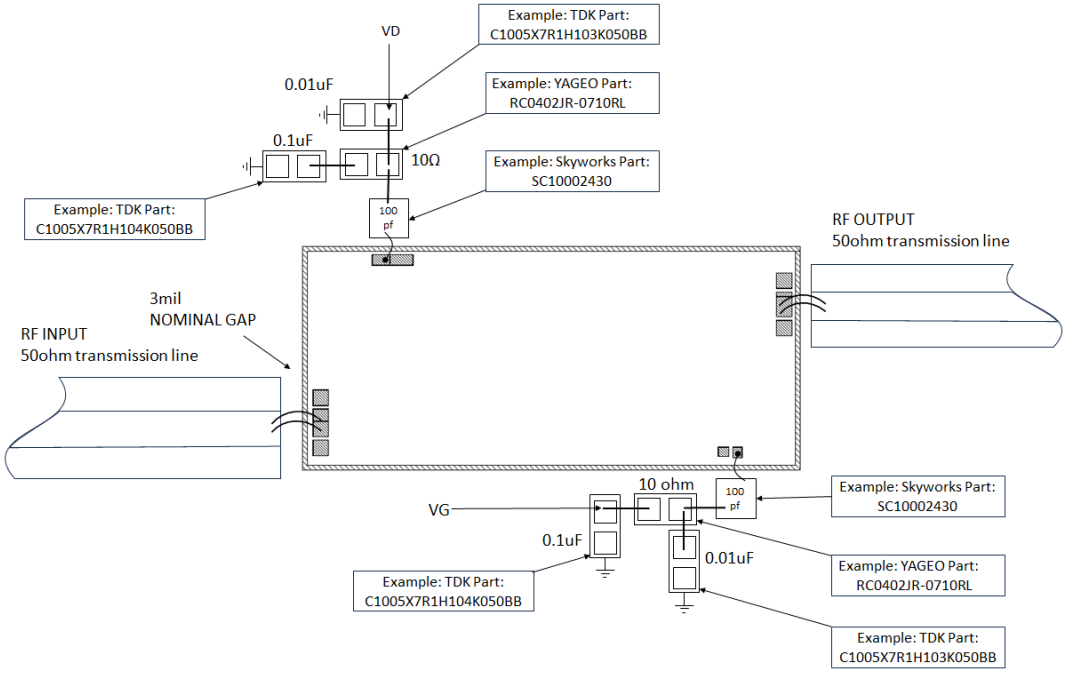
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:
All Dimensions in µm

Notes:

1. **Die thickness: 100µm**
2. **DC bond pad is 100*100µm^2**
3. **RF IN/OUT bond pad is 100*100µm^2**
4. **Bond pad metalization: Gold**
5. **Backside metalization: Gold**

Assembly Drawing



No	Function	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required.
3	VD	Drain Biases for the Amplifier. Connect to external 100pf and 0.1uf bypass capacitors and 10Ω Resistors and 0.01uf capacitors.
4	VG	Gate Biases for the Amplifier. Connect to external 100pf and 0.1uf bypass capacitors and 10Ω Resistors and 0.01uf capacitors.
5	Die Bottom	Die bottom must be connected to RF and dc ground.

Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltage, VG to −3V.
3. Set the drain bias voltages VD to +8V.
4. Increase the gate bias voltages to achieve a quiescent supply current of 110 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to −3V to achieve a I_{DQ} = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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