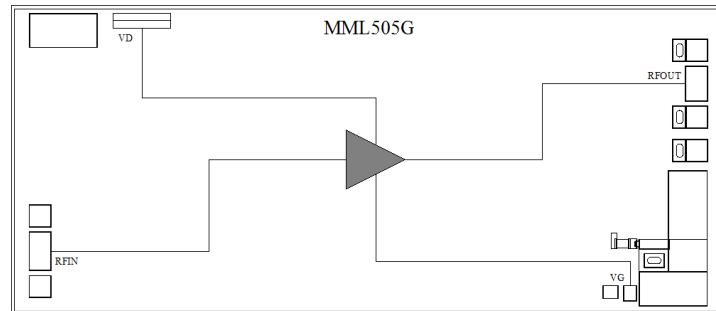


Features

- Frequency: DC-20GHz
- Small Signal Gain: 19.5dB Typical
- Gain Flatness: ± 1.0 dB Typical
- Noise Figure: 2.0dB Typical
- P1dB: 19dBm Typical
- Power Supply: +8V/120mA
- Input/Output: 50 Ω
- Chip Size: 3.18 x 1.38x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

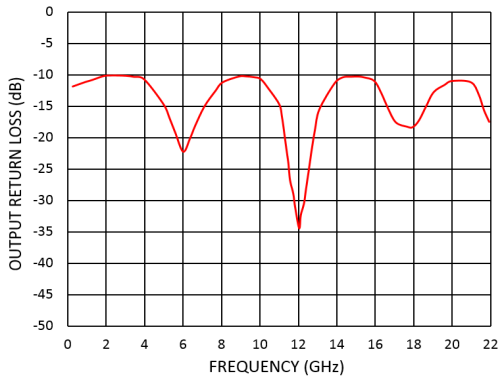
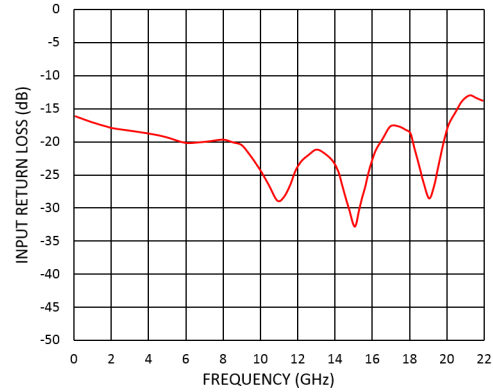
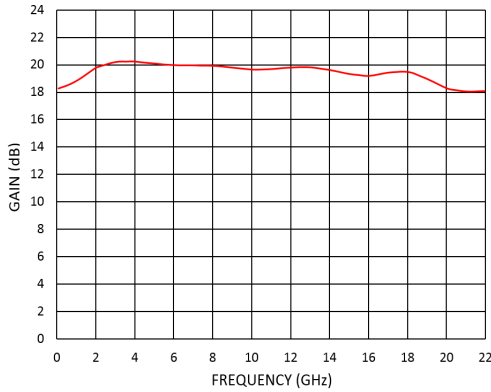
Functional Block Diagram

Electrical Specifications

TA = +25°C, VD = +8V, VG = -0.25V, IDD = 120mA Typical

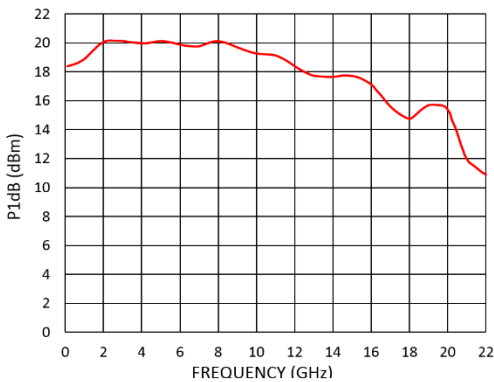
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	DC		12	12		20	GHz
Small Signal Gain	18	19.5		17.5	19		dB
Gain Flatness		± 1.0			± 1.0		dB
Noise Figure		2.0			2.5		dB
P1dB - Output 1dB Compression	17.5	19.5		10	15		dBm
Psat - Saturated Output Power		22.5			18		dBm
OIP3 - Output Third Order Intercept		30			26		dBm
Input Return Loss		17			18		dB
Output Return Loss		10			10		dB



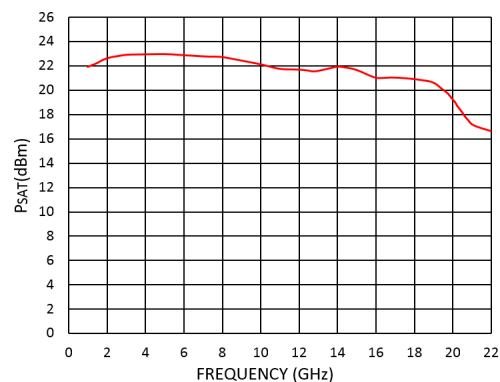
Measurement Plots: S-parameters

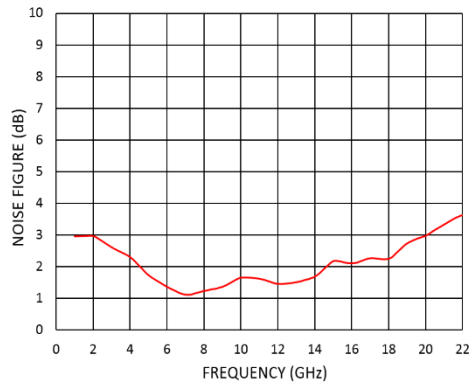


Measurement Plots: P1dB



Measurement Plots: Psat



Measurement Plots: Noise Figure

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+9V
Gate Bias Voltages(VG)	-3V
RF Input Power (RFIN)(VD=+8V)	+23dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 13.3mW/°C above 85 °C)	1.2W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +125 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD

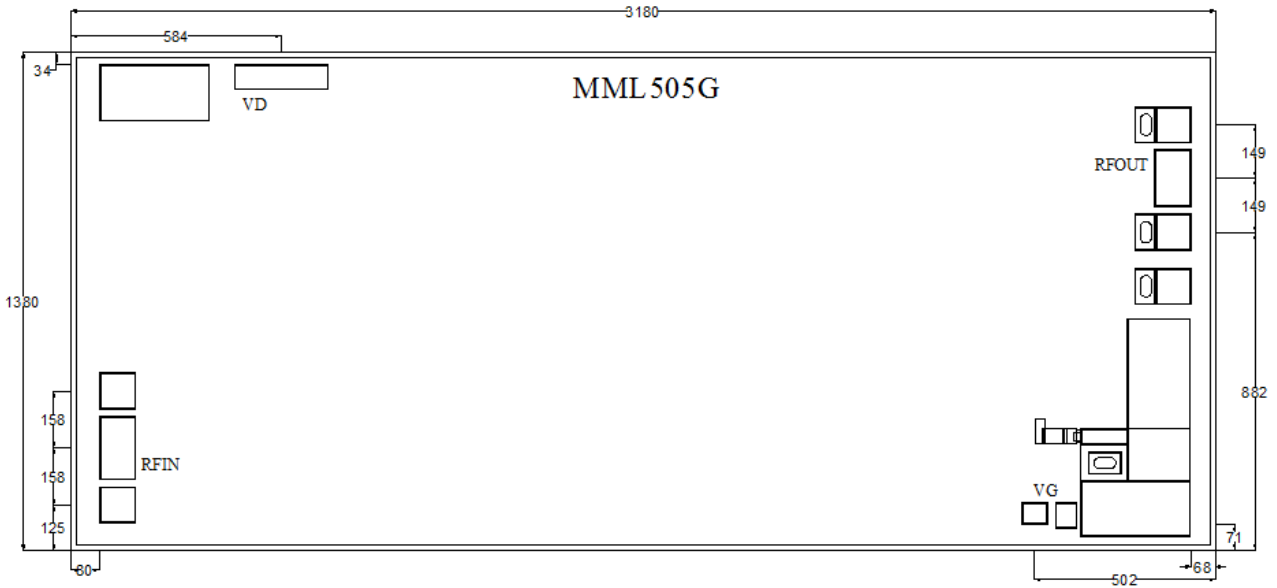
VD (V)	VG (V)	IDD (mA)
+8	-0.25	120



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



Outline Drawing:
All Dimensions in μm

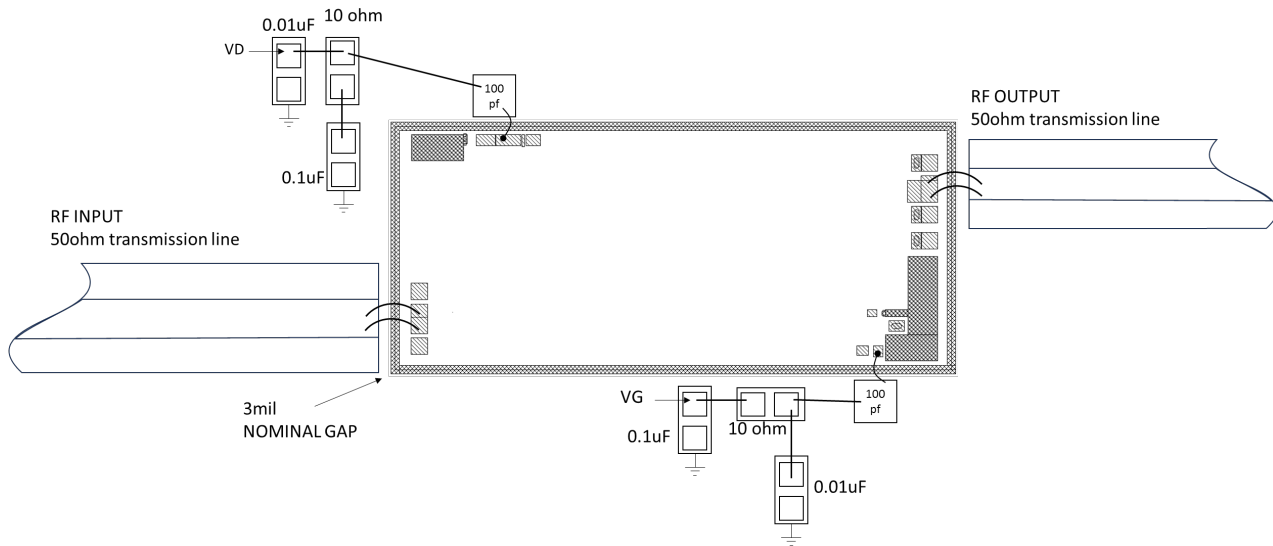


Notes:

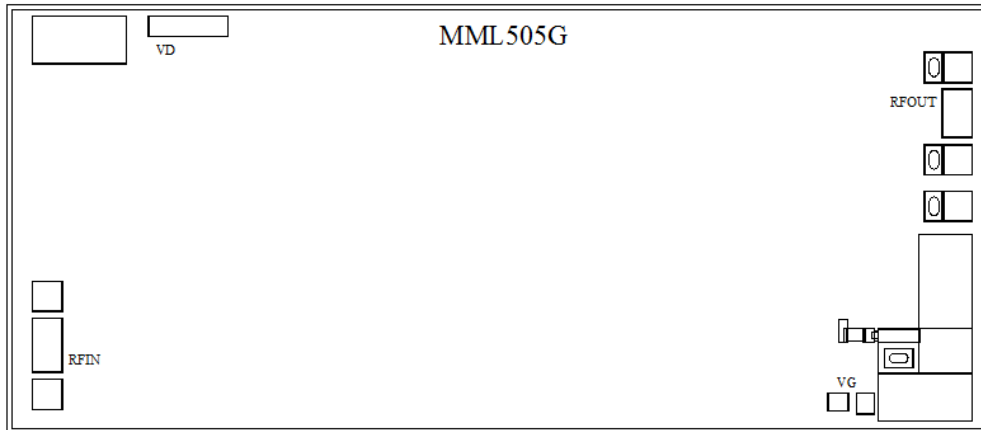
1. Die thickness: 100 μm
2. DC bond pad is 100*100 μm^2
3. RF IN/OUT bond pad is 100*100 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold



Assembly Drawing



No.	Mnemonic	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VD	Drain Biases for the Amplifier. External bypass capacitors of 0.1μf and 0.01 μf and 100 pf are required for these pads.
4	VG	Amplifier 1 st gate bias; External bypass capacitors of 0.1μf and 0.01 μf and 100 pf are required for these pads. ESD protection diodes are included and turn on below -3V.
	Die Bottom	Die bottom must be connected to RF and dc ground.



Biassing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages VG to $-3.0V$.
3. Set the drain bias voltages VD to $+8V$.
4. Increase the gate bias voltages to achieve a quiescent supply current of 120 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to $-3.0V$ to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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