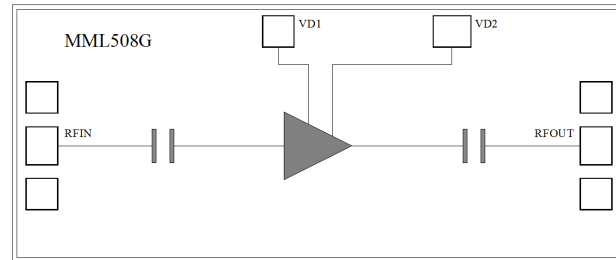




Features

- Single Biasing Voltage (Self Biased)
- Frequency: 18-40GHz
- Small Signal Gain: 23dB Typical
- Gain Flatness: ± 0.3 dB Typical
- Noise Figure: 2.8dB Typical
- P1dB: 15.5dBm Typical
- Power Supply: +5V@74mA
- Input/Output: 50 Ω
- Chip Size: 1.9 x 0.8 x 0.1mm

Functional Block Diagram



Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

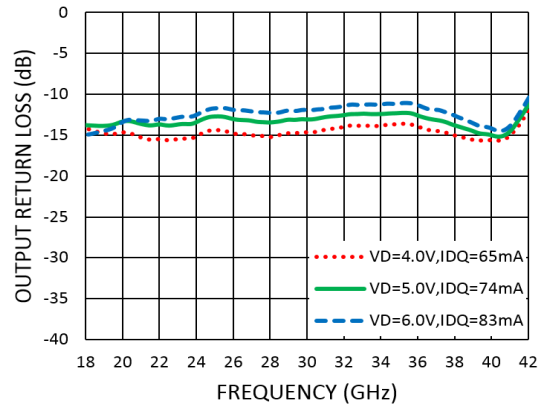
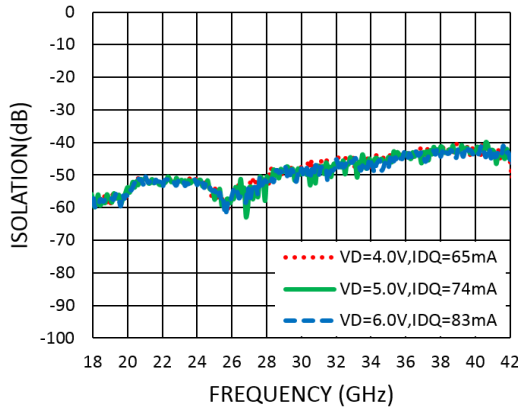
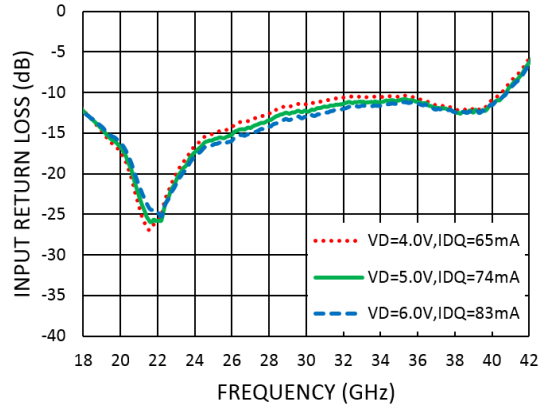
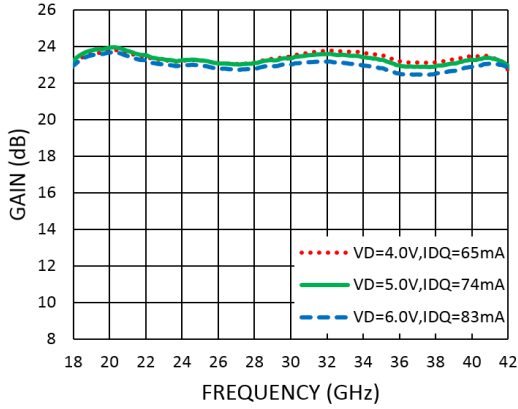
Electrical Specifications

TA = +25°C, VD1&VD2= +5V, IDD = 74mA Typical

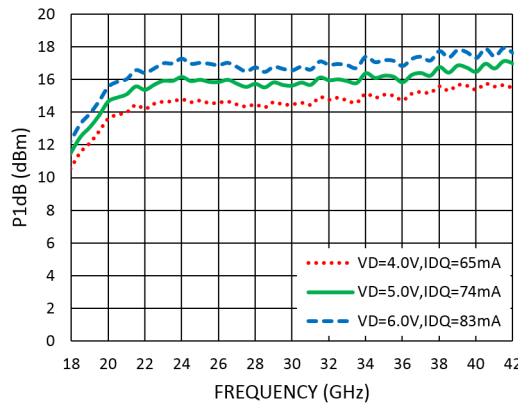
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	18		26	26		40	GHz
Small Signal Gain	21	23		21	23		dB
Gain Flatness		± 0.5			± 0.3		dB
Noise Figure		2.8	3.6		3.5	3.8	dB
P1dB - Output 1dB Compression	10	15		14	15.5		dBm
Psat - Saturated Output Power		17			17.5		dBm
OIP3 - Output Third Order Intercept		26			26		dBm
Input Return Loss		-15			-12		dB
Output Return Loss		-14			-13		dB



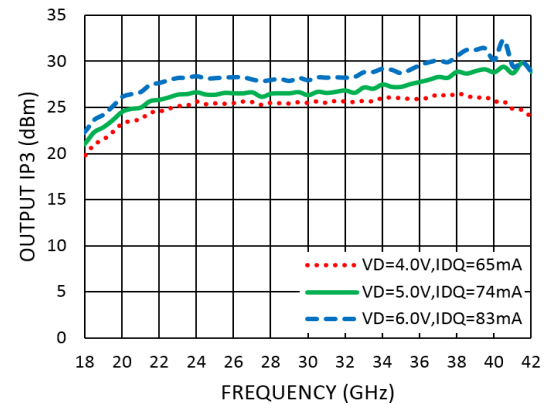
Measurement Plots: S-parameters



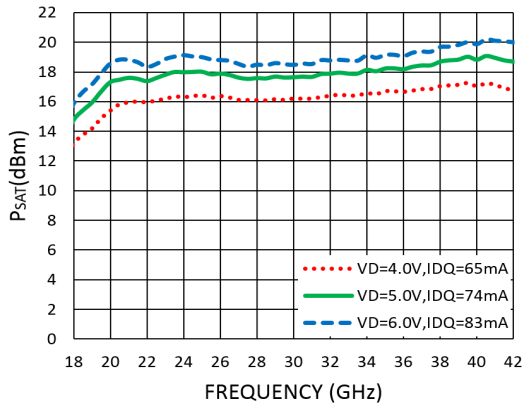
Measurement Plots: P1dB



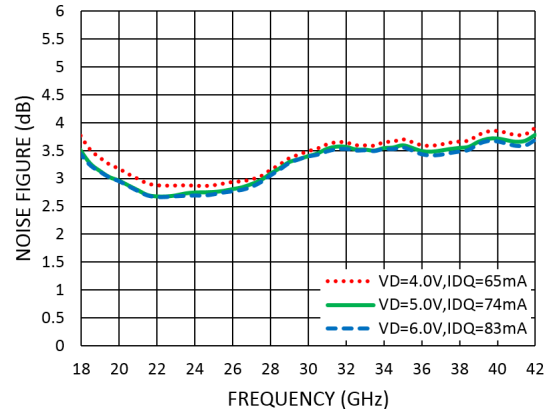
Measurement Plots: OIP3



Measurement Plots: Psat



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+7V
RF Input Power (RFIN)	+15dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 7.2mW/°C above 85 °C)	0.65W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +125 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD

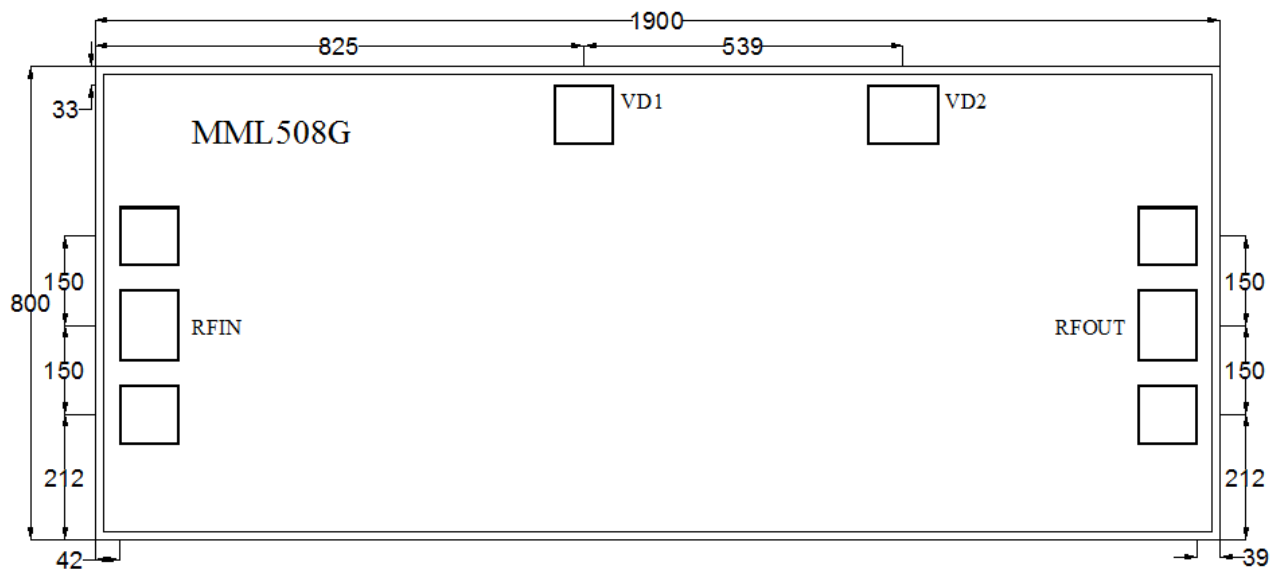
VD (V)	IDD (mA)
+5	74



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



Outline Drawing:
All Dimensions in μm

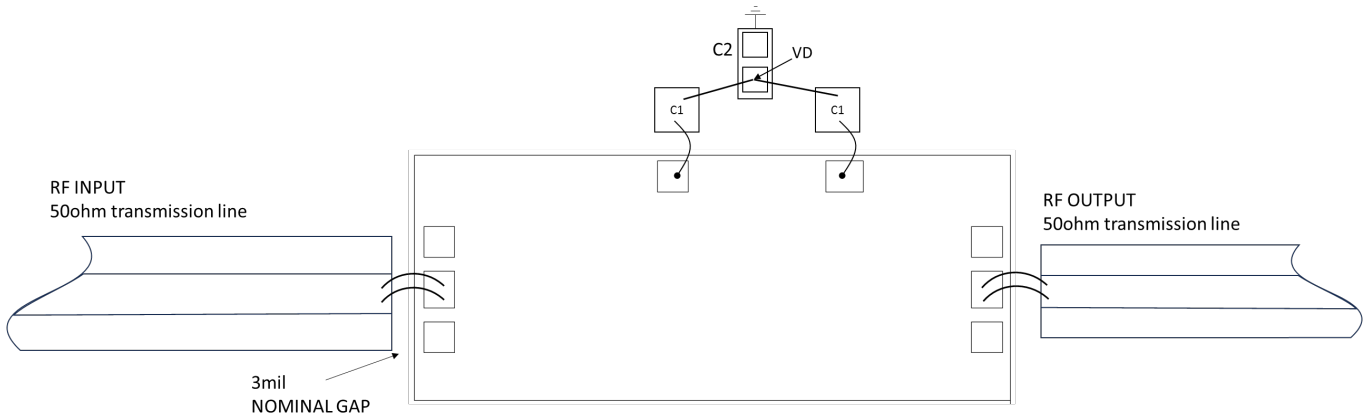


Notes:

1. Die thickness: 100 μm
2. VD1 bond pad is 97*97 μm^2
3. VD2 bond pad is 117*97 μm^2
4. RF IN/OUT bond pad is 97*117 μm^2
5. Bond pad metalization: Gold
6. Backside metalization: Gold

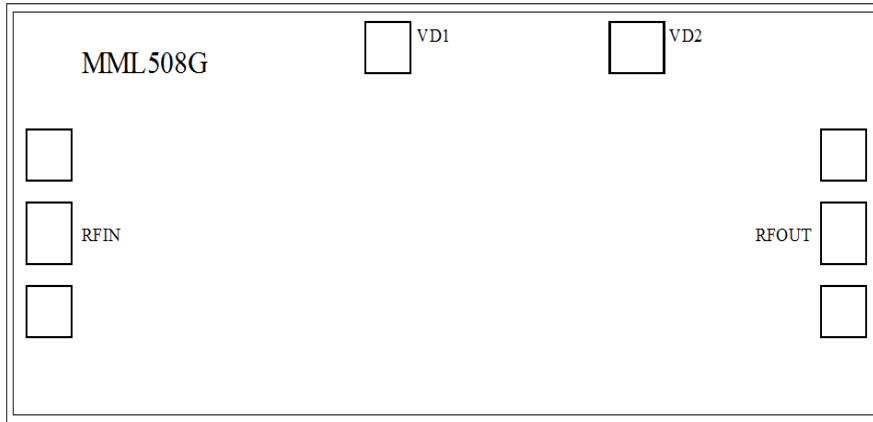


Assembly Drawing



Item	Description
C1	1000 pF Example:KYOCERA AVX Part:116XK102M100TT
C2	10 μ F Example: Murata Electronics Part: GRM188C81C106MA73D (0603)

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD1&VD2	Drain Biases for the Amplifier. External bypass capacitors of 10 μ f and 1000 pf are required for these pads.
4	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Apply positive drain voltage VD1&VD2 and set to +5V .
3. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Turn off the positive drain voltage VD1&VD2.

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