

Features

• Frequency: 45-90GHz

Small Signal Gain: 15dBTypical
Gain Flatness: ±2.0dB Typical
Noise Figure:5.5dB Typical

• P1dB: 12dBm Typical

• Power Supply:

VD=+4V@71mA,VG=-0.5V

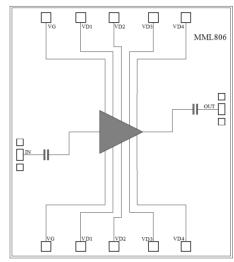
• Input/Output: 50Ω

Chip Size: 1.766 x 2.0 x 0.05mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram



Electrical Specifications

TA = +25°C, VD = +4V, VG=-0.5V, IDD = 71mA Typical

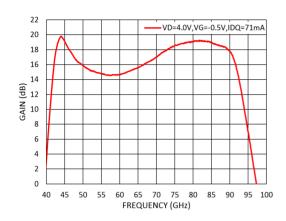
Parameters	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Frequency		45-70		70-90			GHz
Small Signal Gain	14	14 14.5		16	18		dB
Gain Flatness		±1.0			±1.0		dB
Noise Figure		5.5			6.5		dB
P1dB - Output 1dB Compression		11			13		dBm
Psat - Saturated Output Power		13			16		dBm
OIP3 - Output Third Order Intercept		20			22		dBm
Input Return Loss		-18 -13			dB		
Output Return Loss		-13			-18		dB

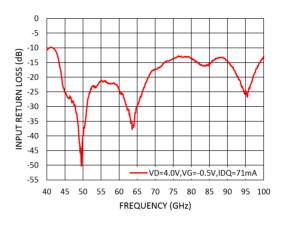
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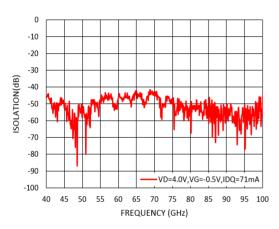
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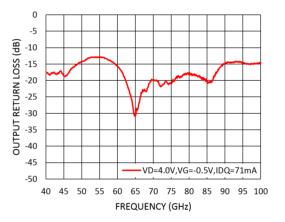


Measurement Plots: S-parameters

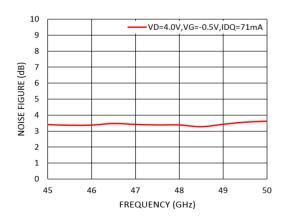








Measurement Plots: Noise Figure



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Absolute Maximum Ratings

Drain Bias Voltage (VD)	+4.5V
Gate Bias Voltage (VG)	-2V to 0V
RF Input Power (RFIN)@(+4V)	+15dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 3.9mW/°C above 85 °C)	0.35W
Thermal Resistance (channel to die bottom)	66°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

VD (V)	VG (V)	IDD (mA)
+4	-0.5	71

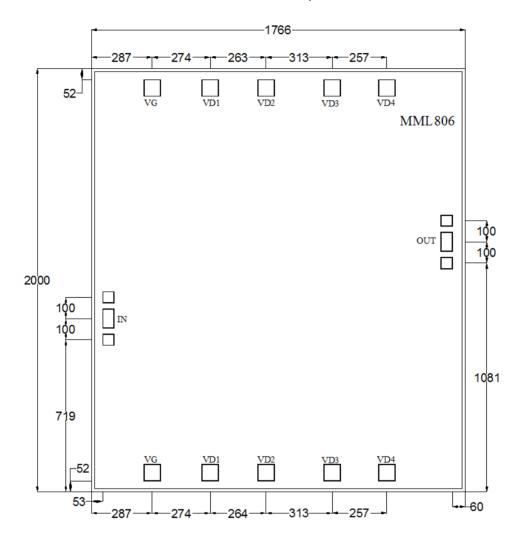


ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS



Outline Drawing:

All Dimensions in µm



Notes:

1. Die thickness: 50µm

2. VD bond pad is 75*75µm²

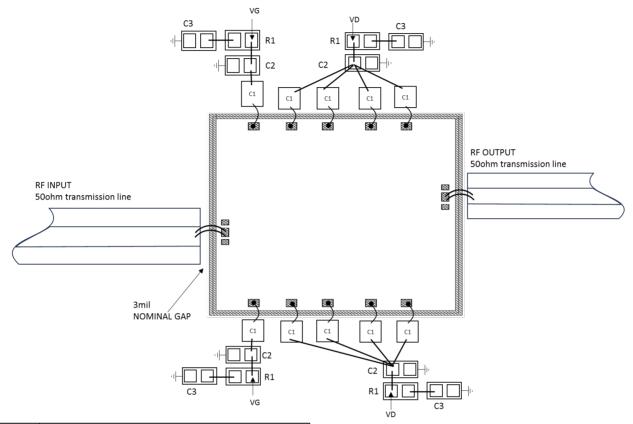
3. VG bond pad is $75*75\mu m^2$

4. RF IN/OUT bond pad is $50*86\mu m^2$

5. Bond pad metalization: Gold 6. Backside metalization: Gold



Assembly Drawing



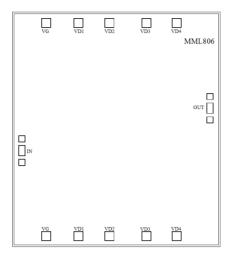
Item	Description		
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1		
C2	0.01µF Example: TDK Part:C1005X7R1H103K050BB (0402)		
C3	0.1μF Example: Murata Electronics Part:GRM033Z71C104KE14D (0201)		
R1	10Ω Example: Yageo Part:RC0201FR-0710RP		

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.

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Biasing and Operation

Turn ON procedure:

- 1. Connect GND to RF and dc ground.
- 2. Set the gate bias voltages, VG to −2V.
- 3. Set the drain bias voltages VD to +4V.
- 4. Increase the gate bias voltages to achieve a quiescent supply current of 71 mA.
- 5. Apply RF signal.

Turn OFF procedure:

- 1. Turn off the RF signal.
- 2. Decrease the gate bias voltages, VG to -2V to achieve a $l_{DQ} = 0$ mA (approximately).
- 3. Decrease the drain bias voltages to 0 V.
- 4. Increase the all gate bias voltages to 0 V.

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