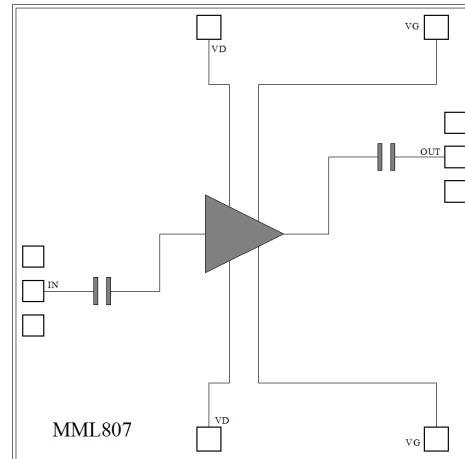


Features

- Frequency: 20-60GHz
- Small Signal Gain: 27dB Typical
- Gain Flatness: ± 2.5 dB Typical
- Noise Figure: 2.8dB Typical
- P1dB: 22dBm Typical
- Power Supply:
VD=+3.5V@83mA, VG=-0.5V
- Input/Output: 50 Ω
- Chip Size: 2.02 x 2.0 x 0.05mm

Typical Applications

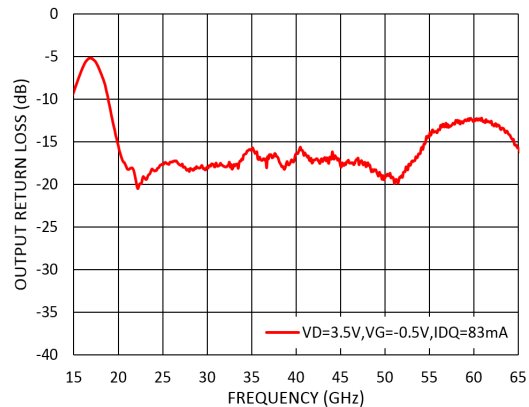
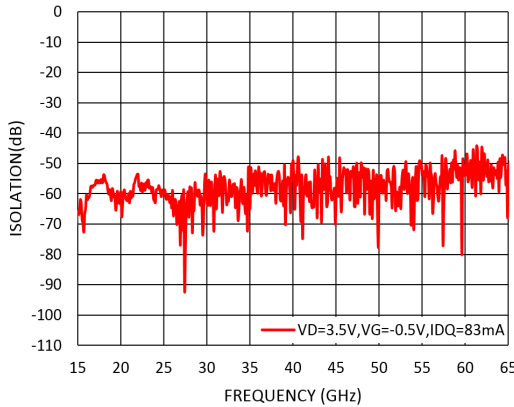
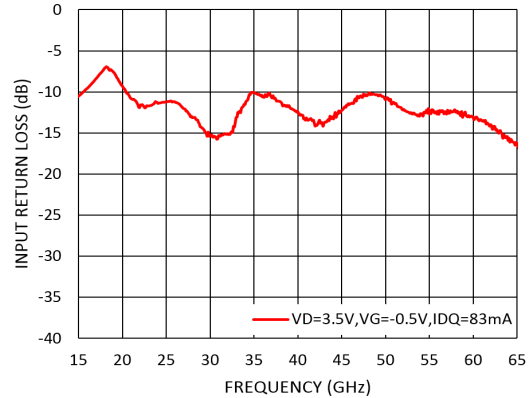
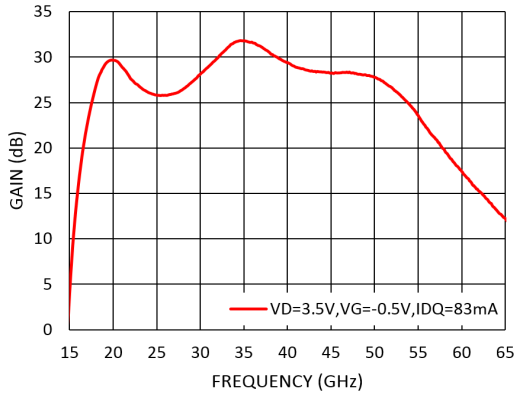
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

Electrical Specifications
TA = +25°C, VD = +3.5V, VG=-0.5V, IDD = 83mA Typical

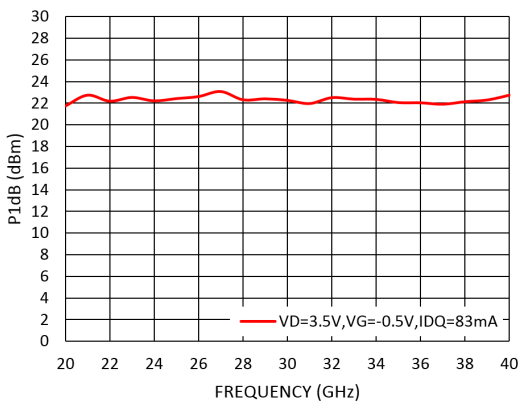
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	20 - 50		50 - 60				GHz
Small Signal Gain	25	27		16	20		dB
Gain Flatness		± 2.5			± 5.0		dB
Noise Figure		2.8	3.8		3.5		dB
P1dB - Output 1dB Compression	20	22			20		dBm
Psat - Saturated Output Power		22.5			21		dBm
OIP3 - Output Third Order Intercept		32			30		dBm
Input Return Loss		-10			-12		dB
Output Return Loss		-17			-14		dB



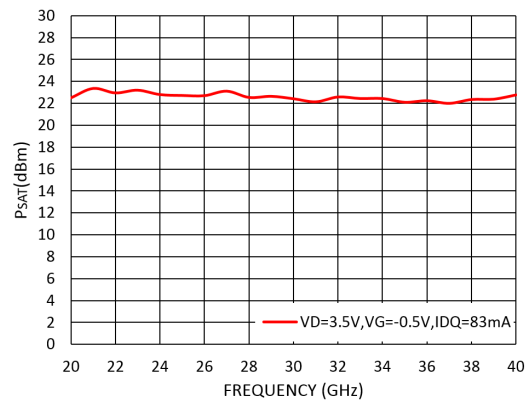
Measurement Plots: S-parameters



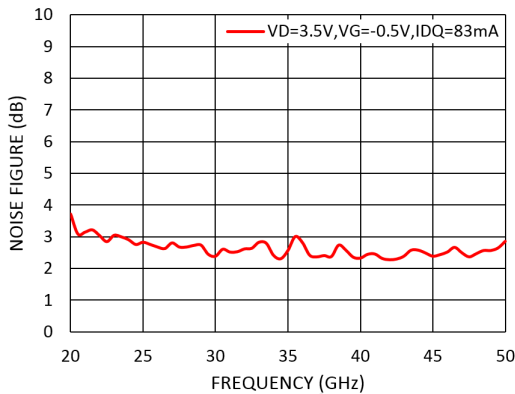
Measurement Plots: P1dB



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+4.5V
Gate Bias Voltage (VG)	-2V to 0V
RF Input Power (RFIN)@(+3.5V)	+5dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 4.6mW/°C above 85 °C)	0.41W
Thermal Resistance (channel to die bottom)	52°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

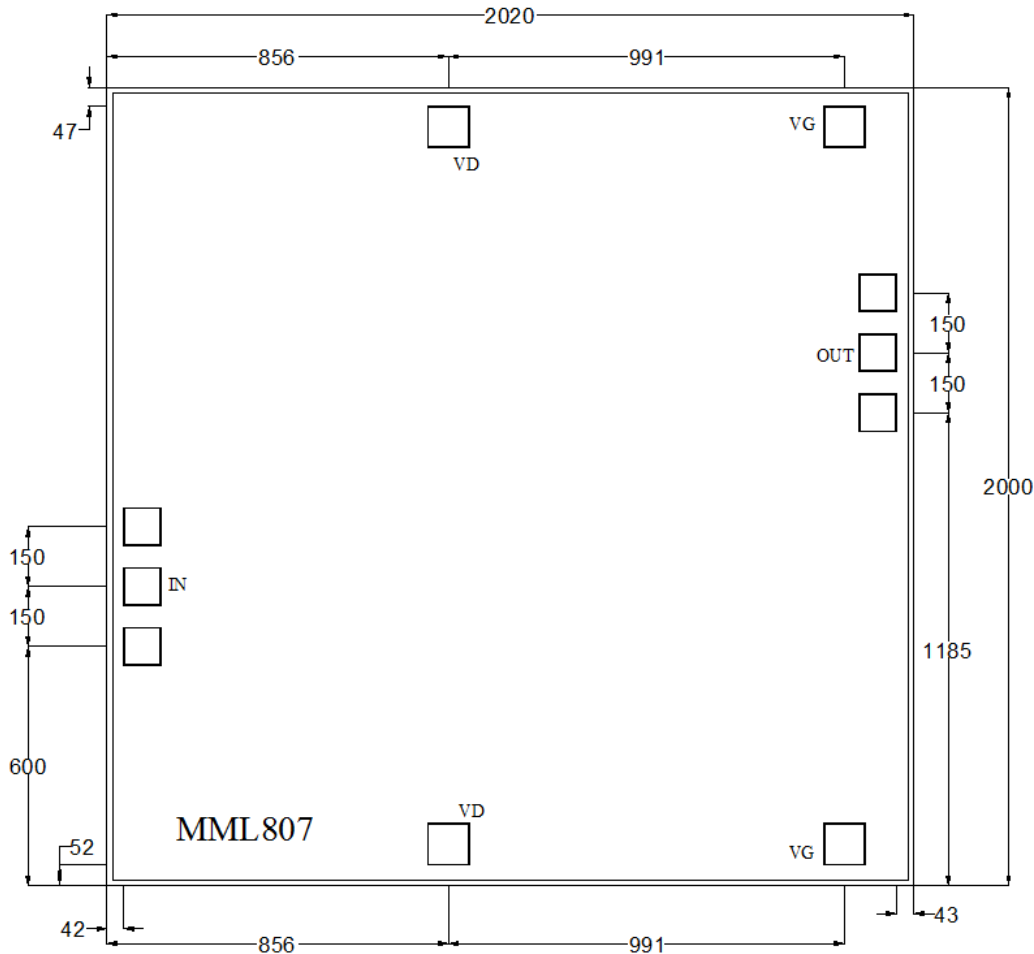
VD (V)	VG (V)	IDD (mA)
+3.5	-0.5	83



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



Outline Drawing: All Dimensions in μm

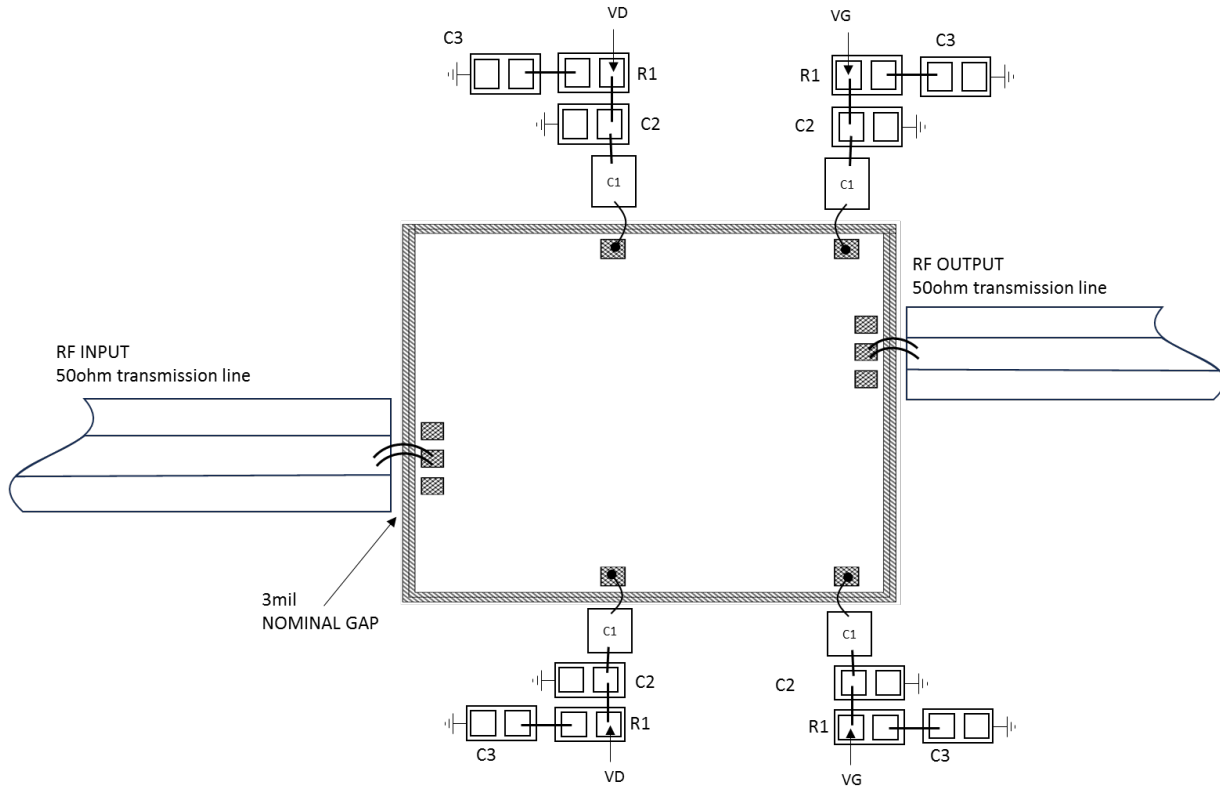


Notes:

1. Die thickness: 50 μm
2. VD bond pad is 100*100 μm^2
3. VG bond pad is 100*100 μm^2
4. RF IN/OUT bond pad is 90*90 μm^2
5. Bond pad metalization: Gold
6. Backside metalization: Gold

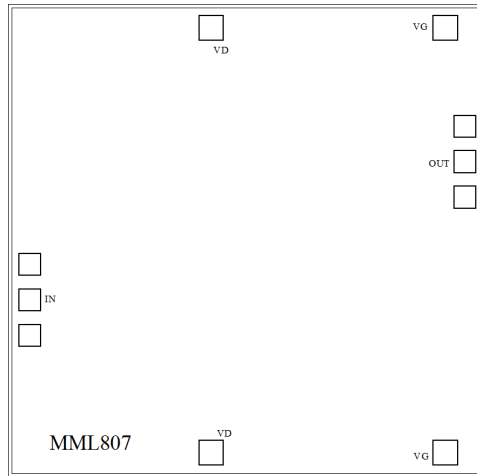


Assembly Drawing



Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1
C2	0.01μF Example: TDK Part: C1005X7R1H103K050BB (0402)
C3	0.1μF Example: Murata Electronics Part: GRM033Z71C104KE14D (0201)
R1	10Ω Example: Yageo Part: RC0201FR-0710RP

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



Biassing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, V_G to $-2V$.
3. Set the drain bias voltages V_D to $+3.5V$.
4. Increase the gate bias voltages to achieve a quiescent supply current of 83 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, V_G to $-2V$ to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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