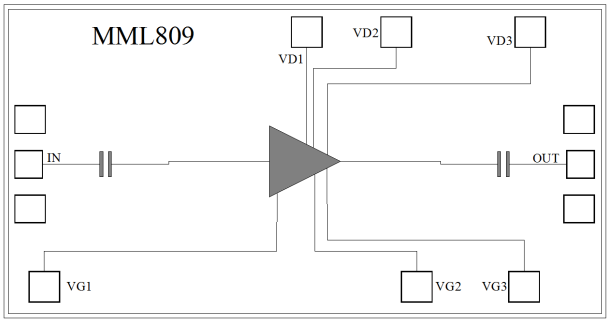
Features

- Frequency: 12-20GHz
- Small Signal Gain: 24dBTypical
- Gain Flatness: ±1.5dB Typical
- Noise Figure:1.3dB Typical
- P1dB: 18dBm Typical
- Power Supply:
  VD=+3.5V@90mA ,VG=-0.5V
- Input/Output: 50Ω
- Chip Size: 2.02 x 1.05 x 0.05mm

Functional Block Diagram



Typical Applications

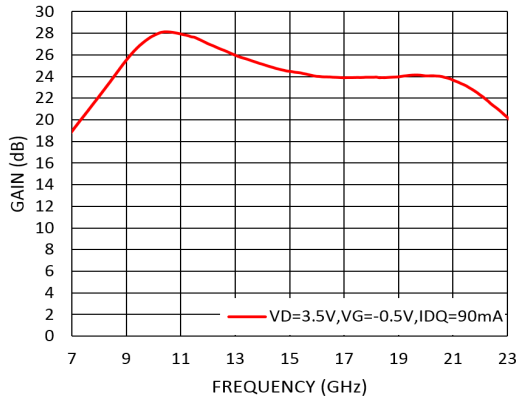
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

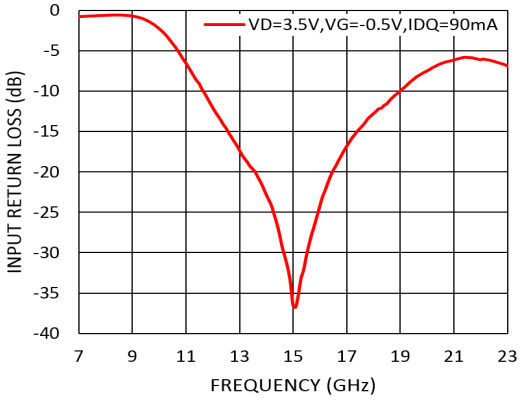
Electrical Specifications

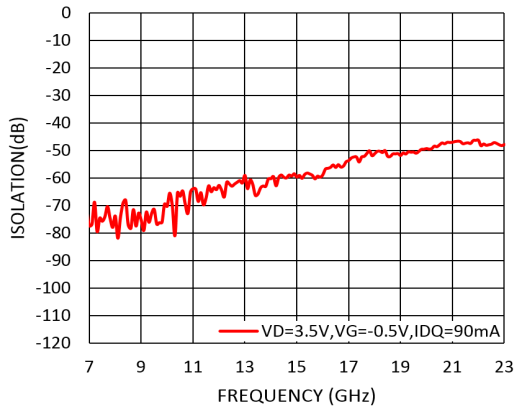
TA = +25°C, VD = +3.5V , VG=-0.5V , IDD = 90mA Typical

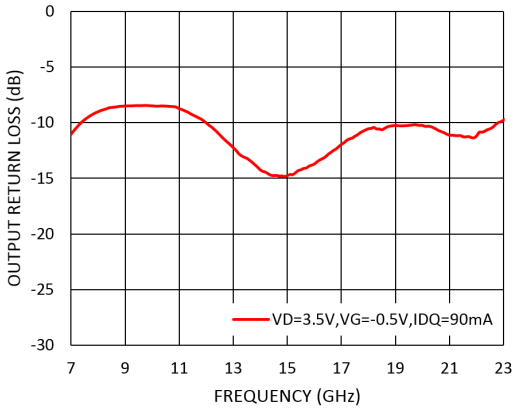
Parameters	Min.	Typ.	Max.	Units
Frequency	12		20	GHz
Small Signal Gain		24		dB
Gain Flatness		±1.0		dB
Noise Figure		1.3	1.6	dB
P1dB - Output 1dB Compression	17	18		dBm
Psat - Saturated Output Power		21		dBm
OIP3 - Output Third Order Intercept		28		dBm
Input Return Loss		-13		dB
Output Return Loss		-10		dB

Measurement Plots: S-parameters

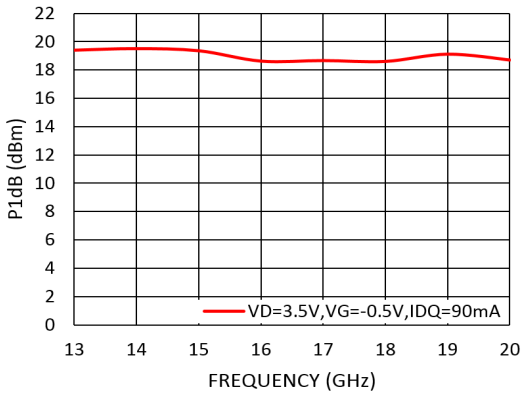




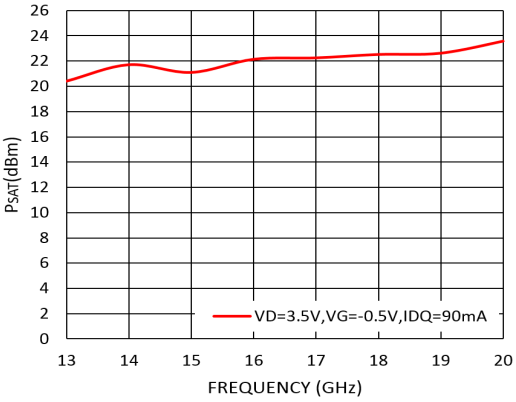




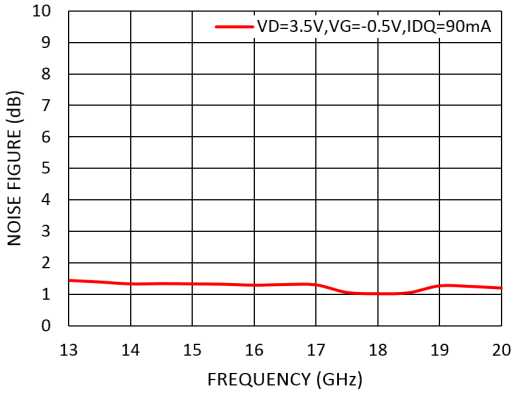
Measurement Plots: P1dB



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+4.5V
Gate Bias Voltage (VG)	-2V to 0V
RF Input Power (RFIN)@(+3.5V)	+15dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 5mW/°C above 85 °C)	0.45W
Thermal Resistance (channel to die bottom)	56°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

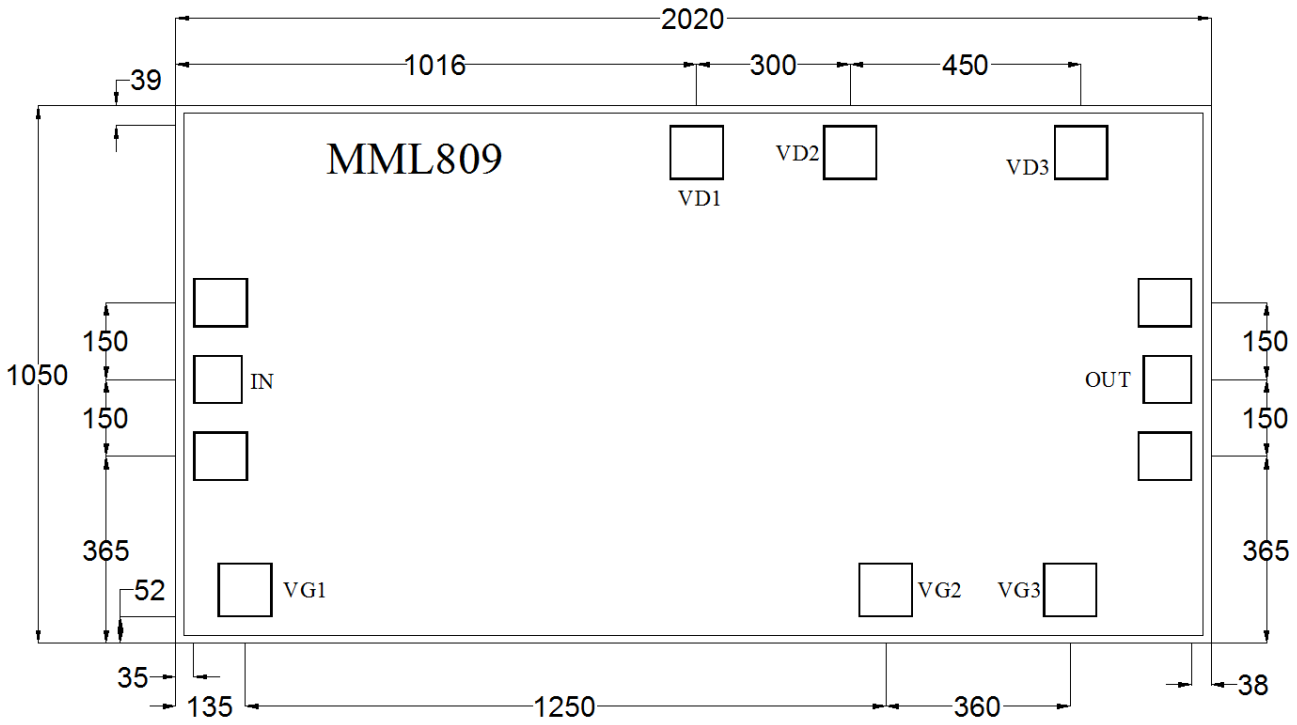
Typical Supply Current vs. VD,VG

VD (V)	VG (V)	IDD (mA)
+3.5	-0.5	90

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:

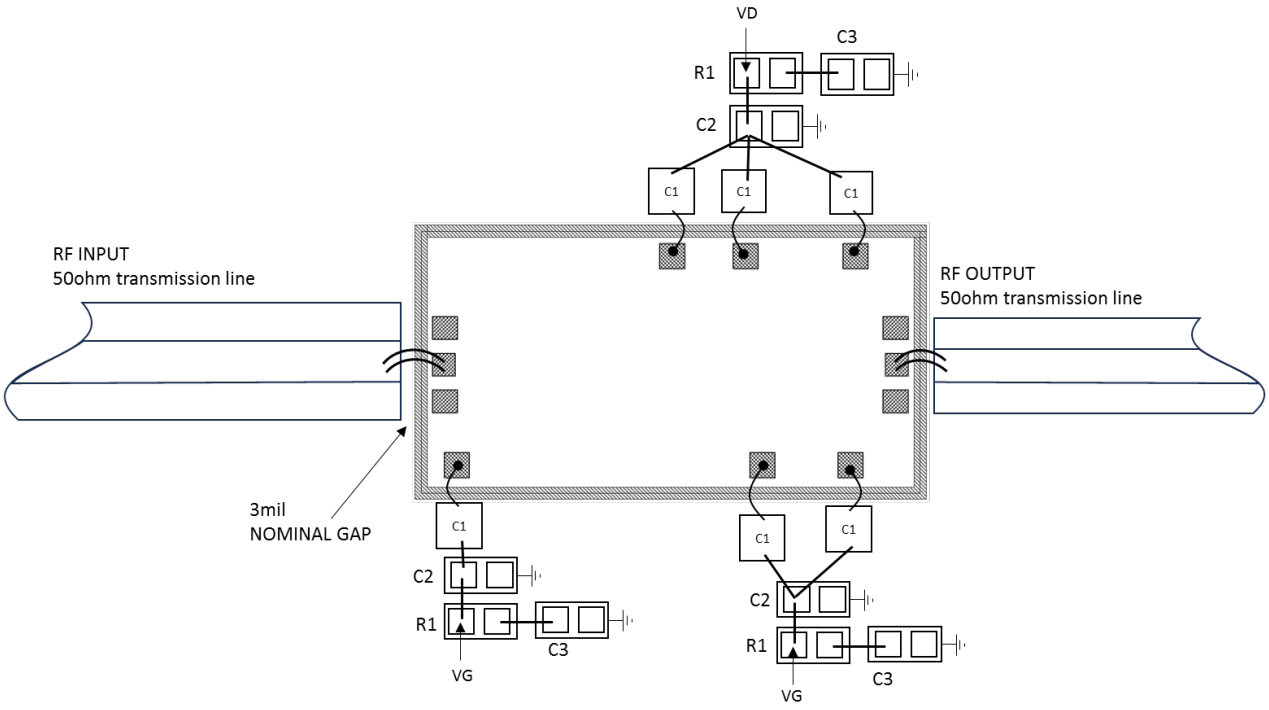
All Dimensions in µm



Notes:

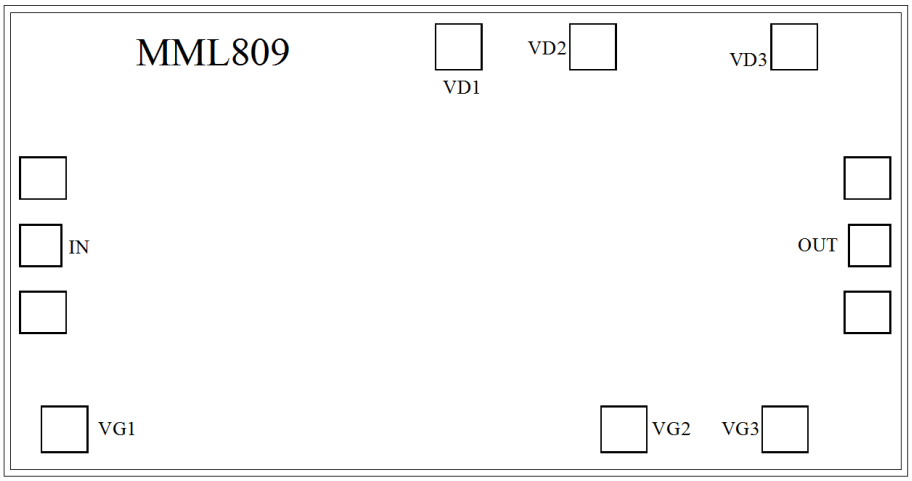
1. Die thickness: 50µm
2. VD bond pad is 100*100µm^2
3. VG bond pad is 100*100µm^2
4. RF IN/OUT bond pad is 90*90µm^2
5. Bond pad metalization: Gold
6. Backside metalization: Gold

Assembly Drawing



Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1
C2	0.01µF Example: TDK Part:C1005X7R1H103K050BB (0402)
C3	0.1µF Example: Murata Electronics Part:GRM033Z71C104KE14D (0201)
R1	10Ω Example: Yageo Part:RC0201FR-0710RP

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages,VG to −2V.
3. Set the drain bias voltages VD to +3.5V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 90 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to −2V to achieve a I_{DQ} = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.