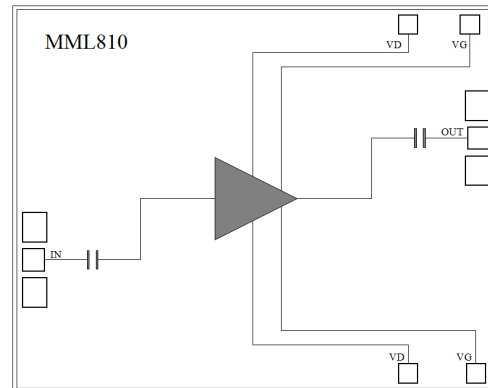


**Features**

- Frequency: 40-75GHz
- Small Signal Gain: 25dB Typical
- Gain Flatness:  $\pm 3.0$ dB Typical
- Noise Figure: 4.0dB Typical
- P1dB: 22dBm Typical
- Power Supply:  
VD=+3.5V@309mA, VG=-0.25V
- Input/Output: 50 $\Omega$
- Chip Size: 2.02 x 1.6 x 0.05mm

**Functional Block Diagram**

**Typical Applications**

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

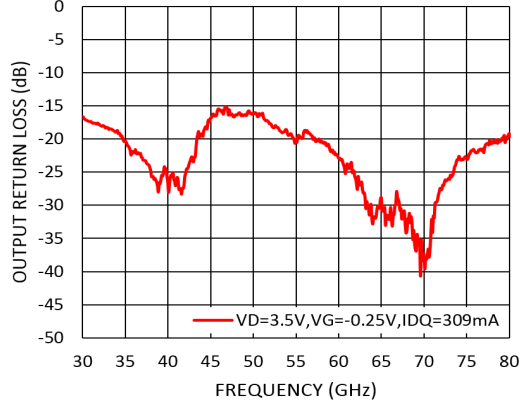
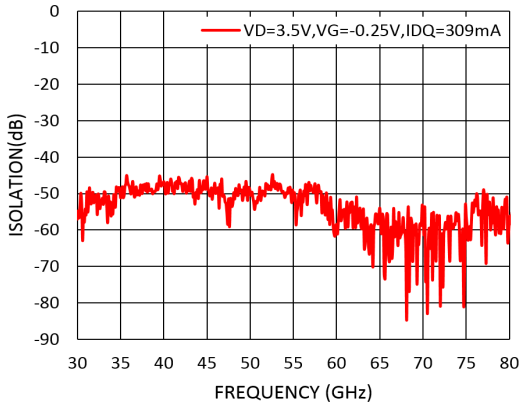
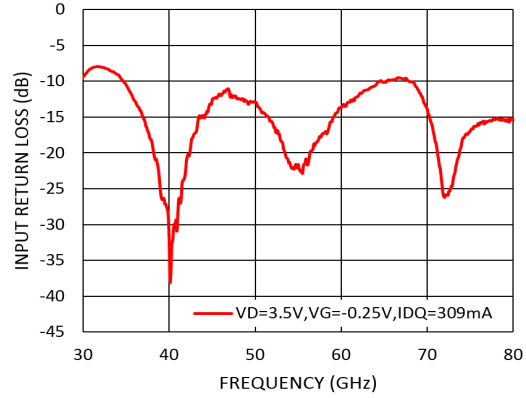
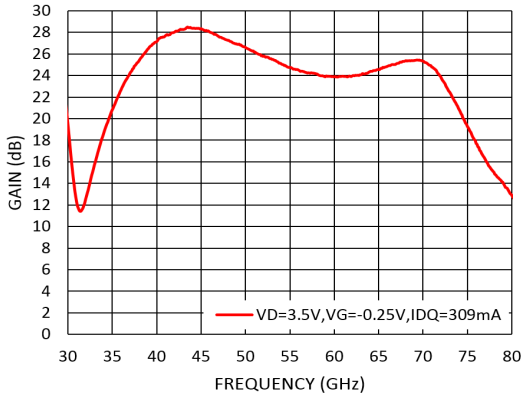
**Electrical Specifications**

TA = +25°C, VD = +3.5V, VG=-0.25V, IDD = 309mA Typical

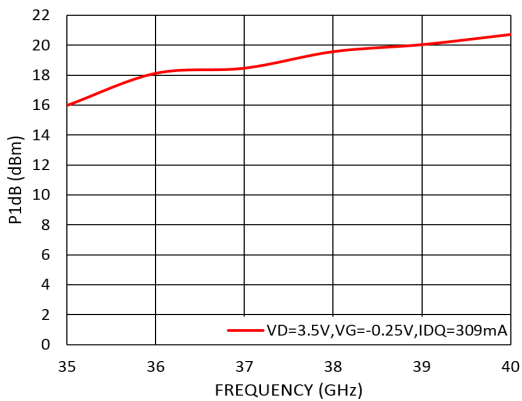
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	40 - 50			50 - 75			GHz
Small Signal Gain	25	27		18	22		dB
Gain Flatness		$\pm 1.0$			$\pm 3.0$		dB
Noise Figure		4.0			4.8		dB
P1dB - Output 1dB Compression		21			22		dBm
Psat - Saturated Output Power		23			24		dBm
OIP3 - Output Third Order Intercept		31			32		dBm
Input Return Loss		-12			-10		dB
Output Return Loss		-15			-20		dB



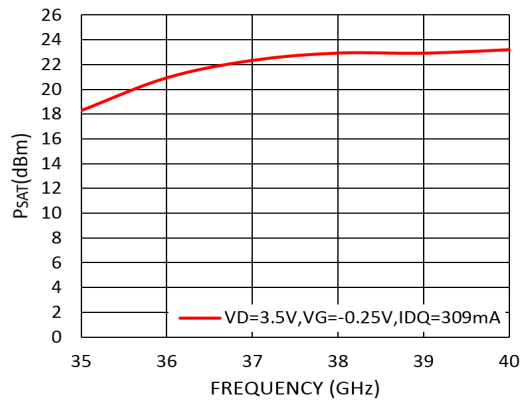
### Measurement Plots: S-parameters



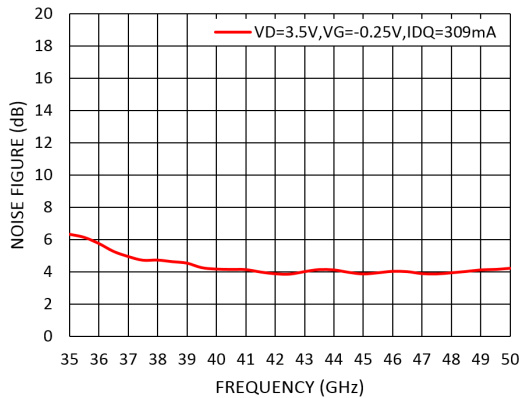
### Measurement Plots: P1dB



### Measurement Plots: PSAT



**Measurement Plots: Noise Figure**



**Absolute Maximum Ratings**

Drain Bias Voltage (VD)	+4.5V
Gate Bias Voltage (VG)	-2V to 0V
RF Input Power (RFIN)@(+3.5V)	+15dBm
Channel Temperature	175°C
Continuous P <sub>diss</sub> (T = 85 °C) (derate 17.8mW/°C above 85 °C)	1.6W
Thermal Resistance (channel to die bottom)	20°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

**Typical Supply Current vs. VD, VG**

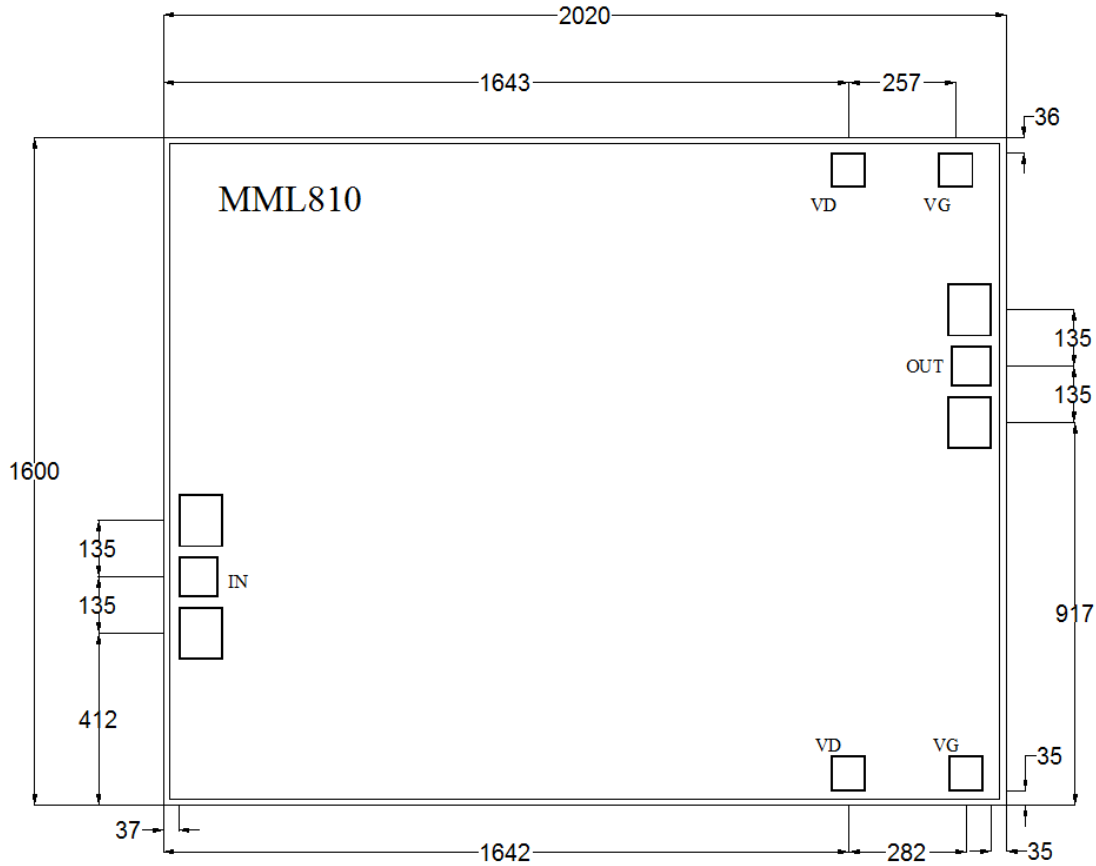
VD (V)	VG (V)	IDD (mA)
+3.5	-0.25	309



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS



**Outline Drawing:**  
All Dimensions in  $\mu\text{m}$

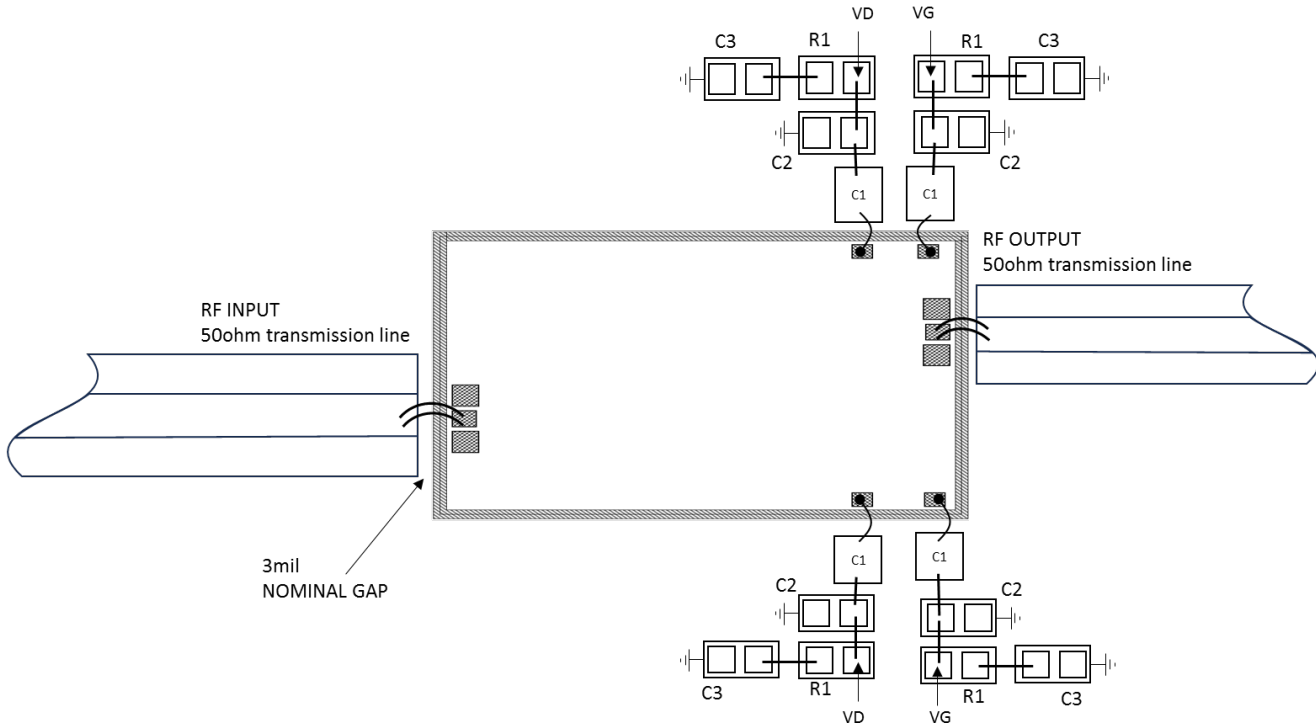


**Notes:**

1. Die thickness: 50 $\mu\text{m}$
2. VD bond pad is 77\*77 $\mu\text{m}^2$
3. VG bond pad is 77\*77 $\mu\text{m}^2$
4. RF IN/OUT bond pad is 90\*90 $\mu\text{m}^2$
5. Bond pad metalization: Gold
6. Backside metalization: Gold

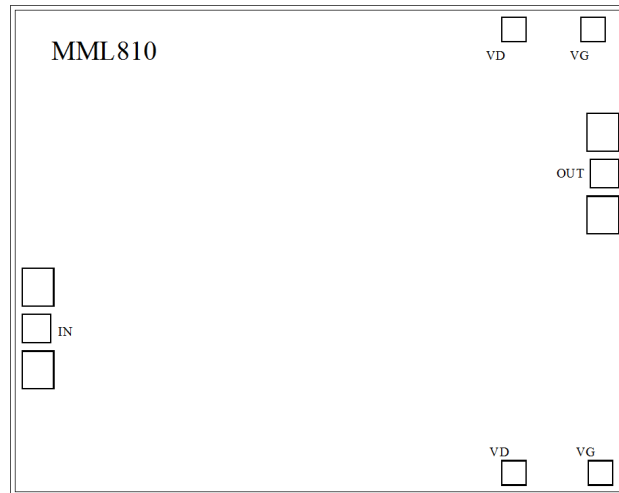


### Assembly Drawing



Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1
C2	0.01μF Example: TDK Part: C1005X7R1H103K050BB (0402)
C3	0.1μF Example: Murata Electronics Part: GRM033Z71C104KE14D (0201)
R1	10Ω Example: Yageo Part: RC0201FR-0710RP

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



## Biassing and Operation

### Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VG to  $-2V$ .
3. Set the drain bias voltages VD to  $+3.5V$ .
4. Increase the gate bias voltages to achieve a quiescent supply current of 309 mA.
5. Apply RF signal.

### Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to  $-2V$  to achieve a  $I_{DQ} = 0$  mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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