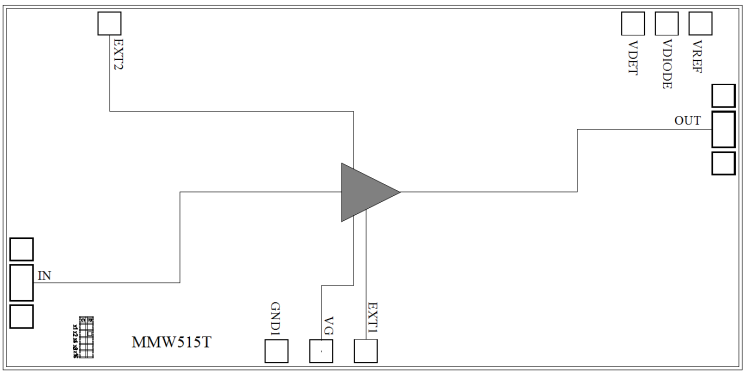
Features

- Frequency: DC-24GHz
- Small Signal Gain: 20dB Typical
- Gain Flatness: ±1.5dB Typical
- Noise Figure: 2.5dB Typical
- Psat: 31dBm Typical @ +12V/-0.45V
- Supply voltage:
  VD =+12V
  VG=-0.45V
- Input/Output: 50Ω
- Die Size: 3.3 x 1.63 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

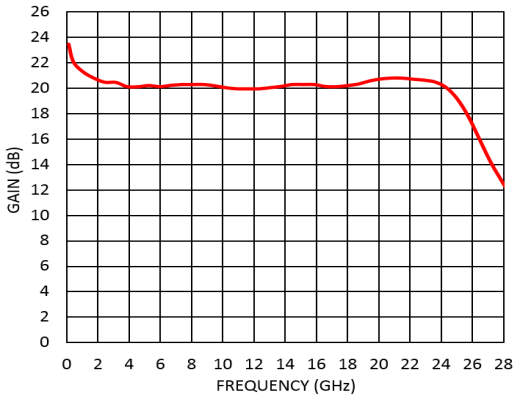


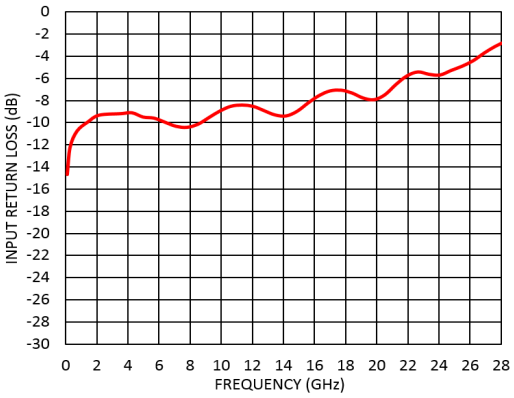
Electrical Specifications

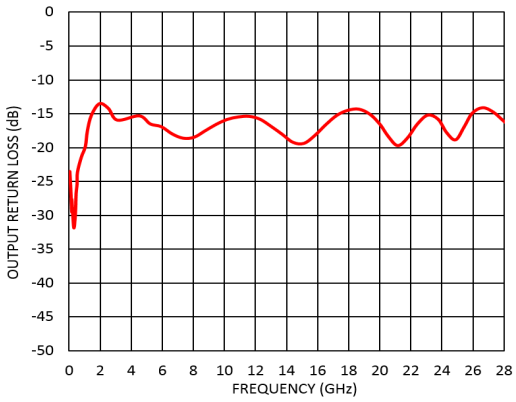
TA = +25°C, VD=+12V,VG= -0.45V IDD = 443mA Typical

Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	DC		10	10		24	GHz
Small Signal Gain	18	20		18	20		dB
Gain Flatness		±1.5			±0.5		dB
Noise Figure		2.5			4		dB
P1dB - Output 1dB Compression		29			28		dBm
Psat - Saturated Output Power		31			29.5		dBm
Input Return Loss		9			7		dB
Output Return Loss		15			15		dB
* Adjust VG slightly to obtain device current of 443 mA.							

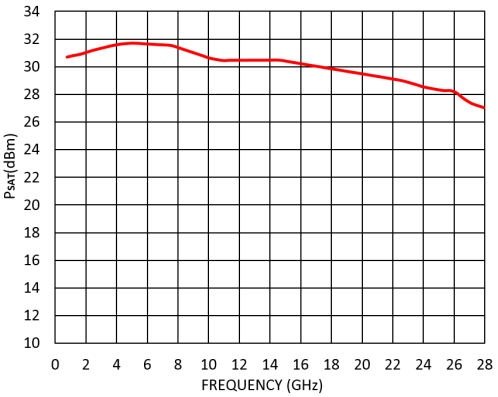
Measurement Plots: S-parameters



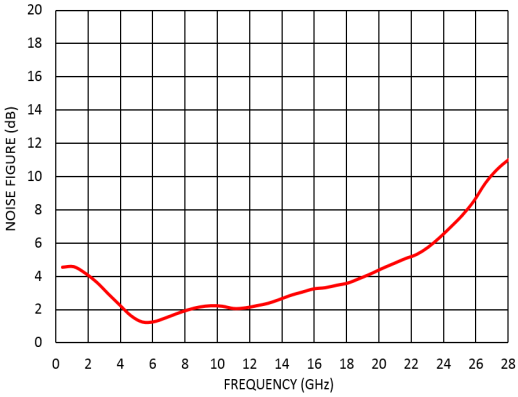




Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+14V
Gate Bias Voltages(VG)	–1 to 0 V
RF Input Power (RFIN)@(+12V)	+16dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 78mW/°C above 85 °C)	7W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

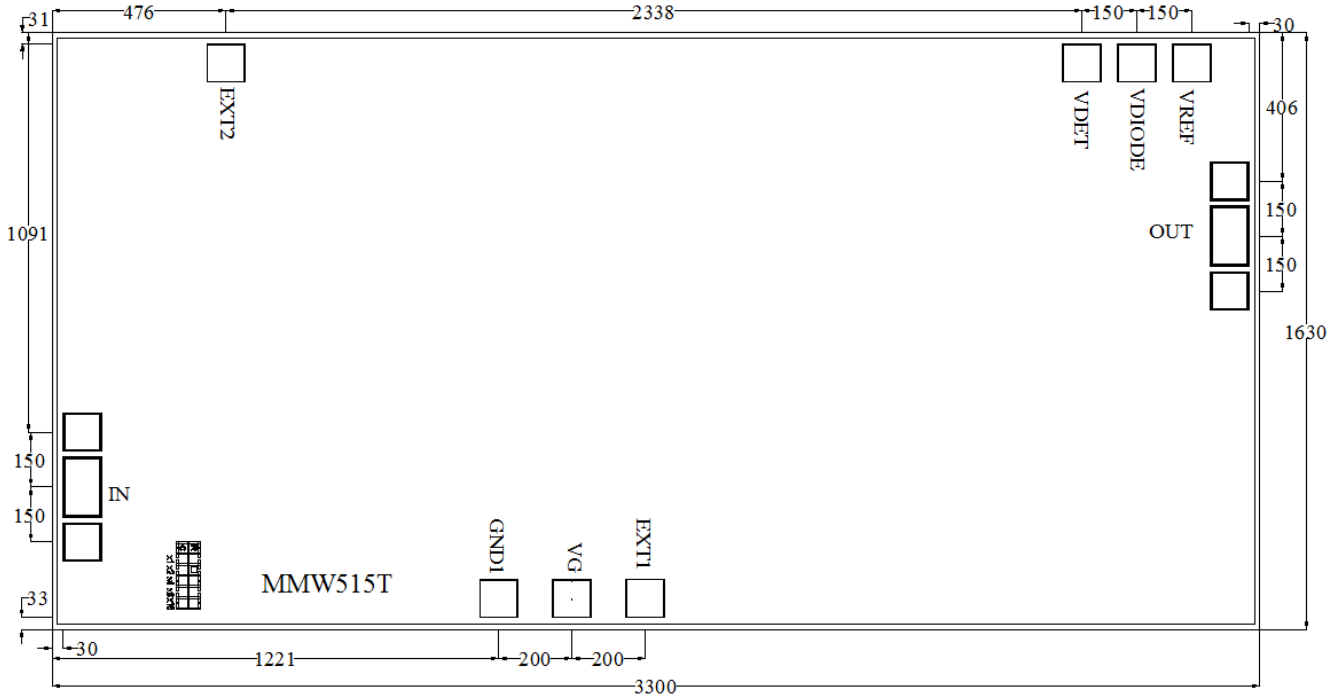
Typical Supply Current vs. VD,VG

VD (V)	VG (V)	IDD (mA)
12	-0.45	443

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:

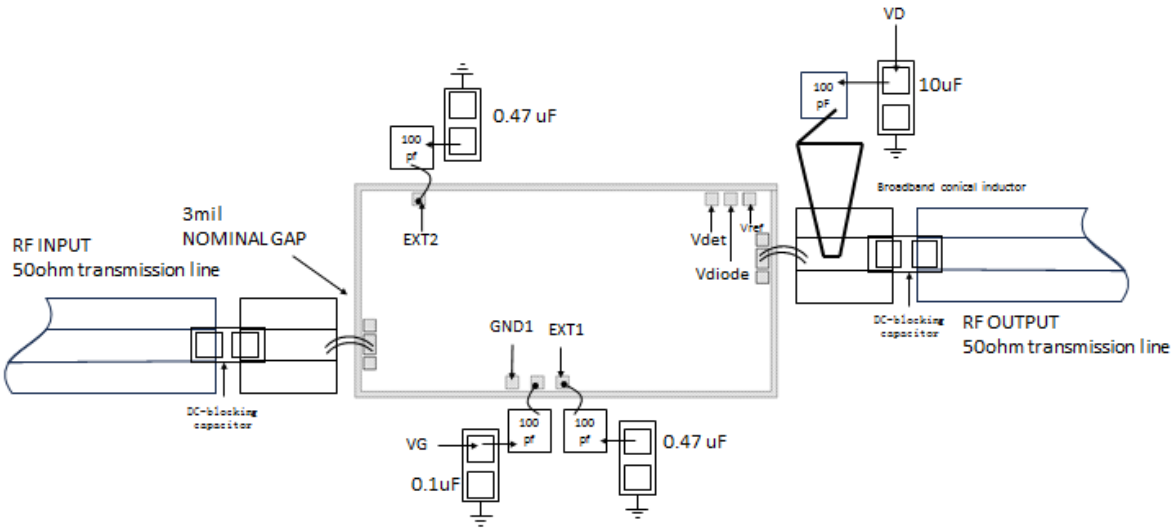
All Dimensions in μm



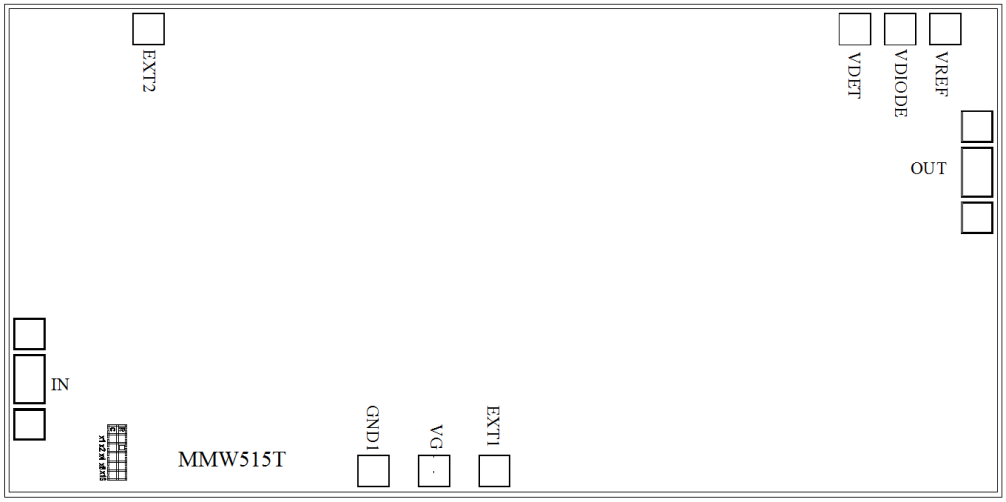
Notes:

1. **Die thickness: 100μm**
2. **DC bond pad is 100*100μm²**
3. **RF IN/OUT bond pad is 100*100μm²**
4. **Bond pad metalization: Gold**
5. **Backside metalization: Gold**

Assembly Drawing



No.	Mnemonic	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VG	Amplifier Gate Controls. External bypass capacitors of 0.1µf and 100pf are required for these pads. ESD protection diodes are included and turn on below −1.0 V.
4	EXT1	External bypass pad; connect to external 100pf and 0.47uf bypass capacitor.
5	EXT2	External bypass pad; connect to external 100pf and 0.47uf bypass capacitor.
6	Vref	Detector ref
7	Vdiode	Detector bias
8	Vdet	Detector output
9	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages,VG1 to −1.0V.
3. Set the drain bias voltages VD to +12V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 443 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1 to −1.0V to achieve a I_{DQ} = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.