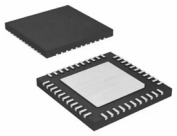
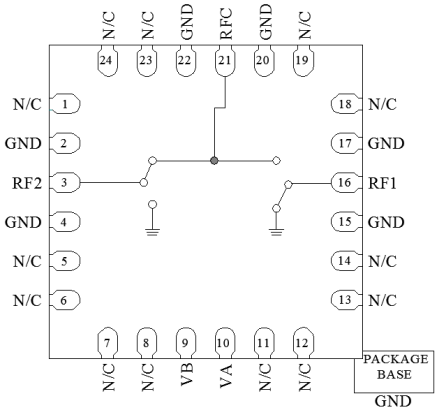
Features

- SP2T Reflective design
- Frequency: 8-12GHz
- P0.3dB: 47dBm Typical
- Insertion Loss: 0.8dB Typical
- Control Voltage:0/-40V
- Switching Speed: 20ns Typical
- Package Size : 4 x 4 x 0.75mm



Functional Block Diagram



Typical Applications

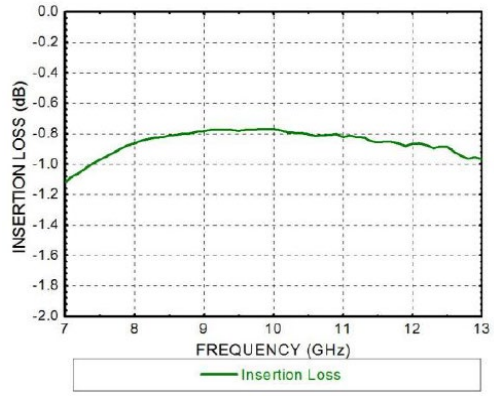
- Voltage control
- Fast Switching Speed
- Low Insertion Loss and High Isolation
- Customization available upon request

Electrical Specifications

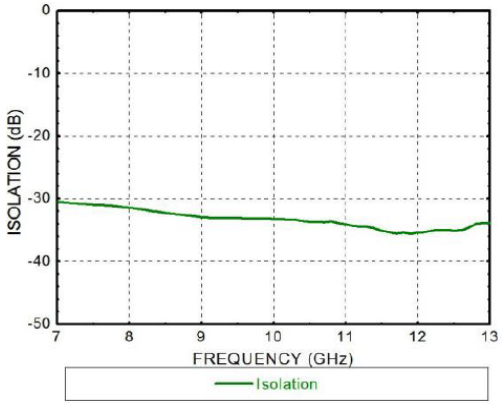
TA = +25°C, VCTL = 0/-40V

Parameters	Min.	Typ.	Max.	Units
Frequency	**8**		**12**	**GHz**
Insertion Loss		**0.8**		**dB**
Isolation		**33**		**dB**
Input Return Loss		**-18**		**dB**
Output Return Loss		**-23**		**dB**
P0.3dB - Output 0.3dB Compression		**47**		**dBm**
IIP3-Input Third Order Intercept		**/**		**dBm**
Switching Speed		**20**		**ns**

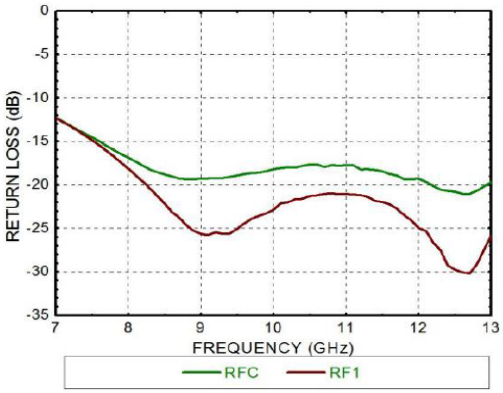
Insertion Loss vs. Frequency



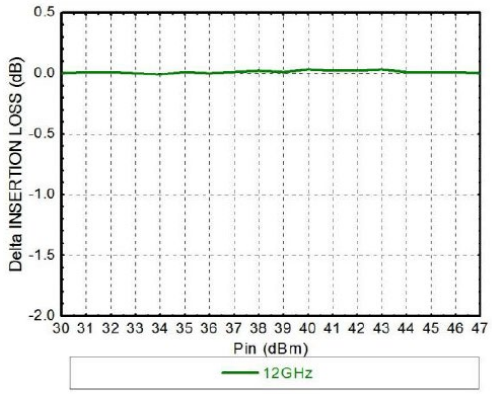
Isolation vs. Frequency



Return Loss vs. Frequency(ON State)

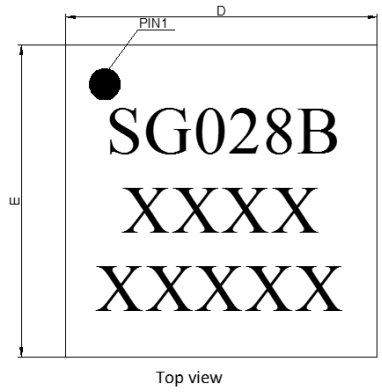


Insertion Loss Compression vs Input Power (Normalized)

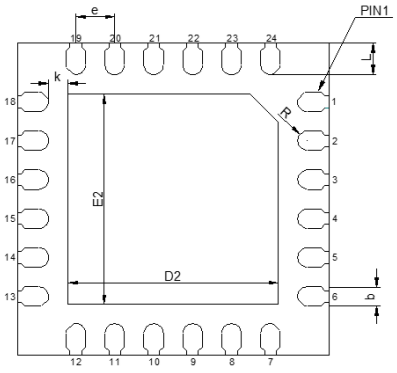


Outline Drawing:

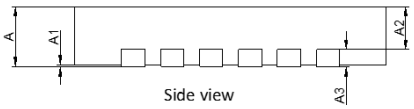
All Dimensions in mm



Top view



Bottom view



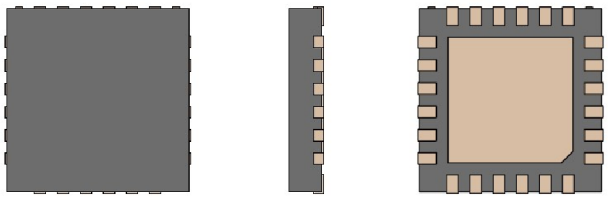
Side view

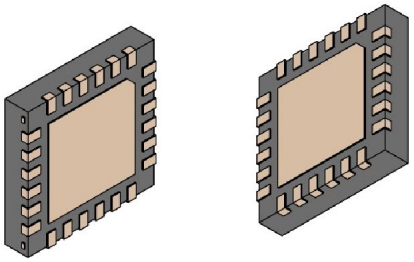
UNITS=MM

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.035	0.05
A2	--	0.55	--
A3	--	0.20	--
D	3.90	4.00	4.10
E	3.90	4.00	4.10
b	0.20	0.25	0.30
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50	
K	0.20		
L	0.35	0.40	0.45
R	0.10		

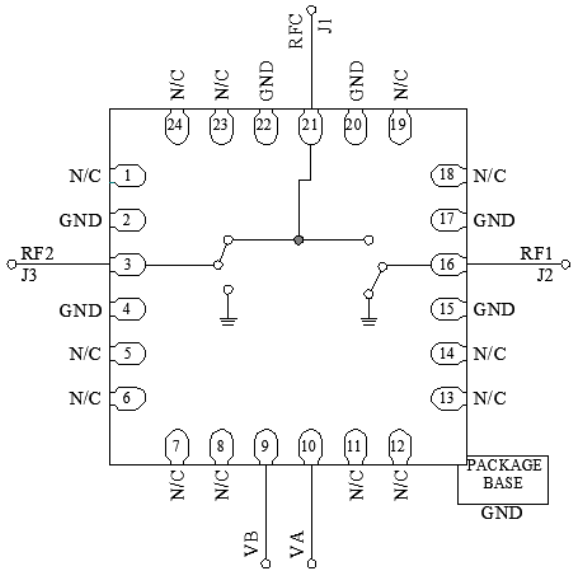
Notes:

1. **Package model : 24-Lead Lead Frame Chip Scale Package .**
2. **Dimensions are in millimeters.**
3. **Lead spacing tolerance is non-cumulative.**





Assembly Drawing



Pin Descriptions

No	Function	Description
1,5,6,7,8,11,12,13,14, 18,19,23,24	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
2,4,15,17,20,22	GND	Connected to RF/DC ground.
21	RFC	Signal input terminal, connected to 50Ω circuit.
3,16	RF1,RF2	Signal output terminal, connected to 50Ω circuit.
9	VB	Control terminal, connected to 0 or -40V.
10	VA	Control terminal, connected to 0 or -40V.
25	GND	Package bottom must be connected to RF/DC ground.

Truth Table

Function	A	B
RFC-RF1	-40V	0V
RFC-RF2	0V	-40V

Absolute Maximum Ratings

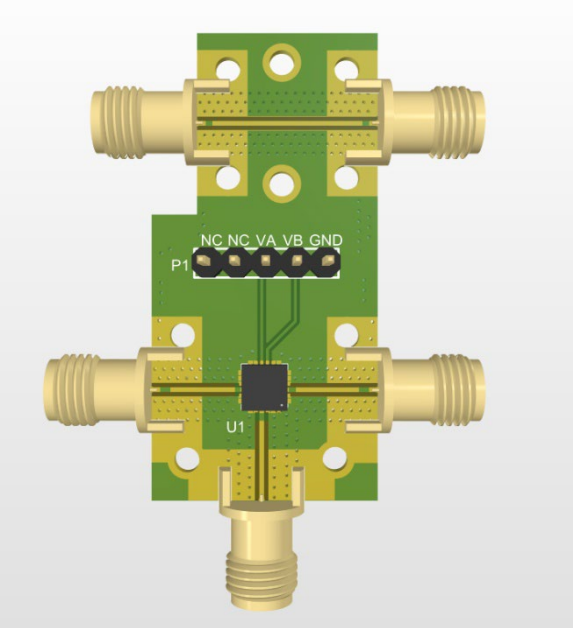
RF Input Power (RFIN)	**+48dBm**
Control Voltage	**-50V**
Control Current	**2mA**
Channel Temperature, TCH	**175°C**
Thermal Resistance (Junction-to-Case (θJC) (1)	**5.5°C/W**
Operating Temperature	**-55°C to +85°C**
Storage Temperature	**-65°C to +150°C**

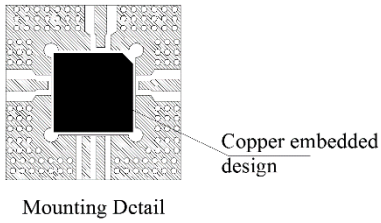
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Notes:

1. Thermal resistance is referenced to the back of the package.

Evaluation Board Layout Assembly and Mounting Pattern





Mounting Detail

Top dielectric material is ROGERS 4003C, 0.008 inch thickness with 0.5 oz copper.

The pad pattern shown above has been developed and tested for optimized assembly at Miller. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

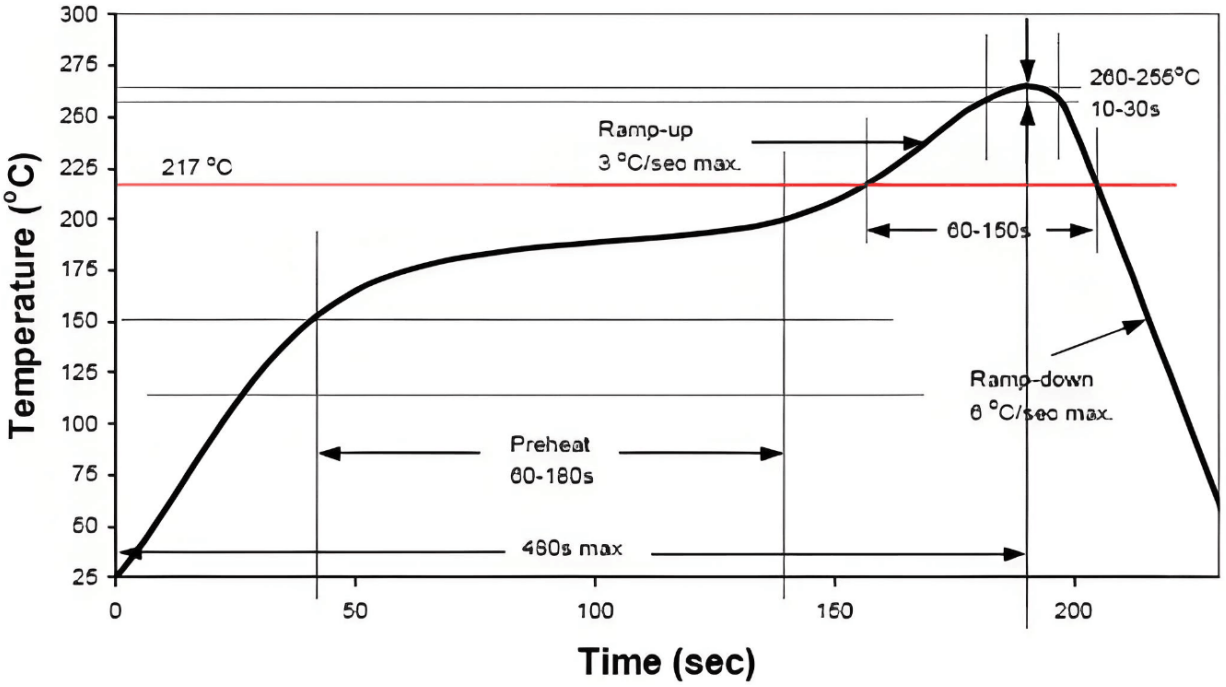
Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008~0.01 in. diameter drill, filled with copper plating.

The bottom of the IC adopts a copper embedded design to ensure good heat transfer, and the copper surface maintains the same height as the PCB substrate.

Solderability

1. Compatible with lead-free soldering process with 260 ℃ peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile



Pre-Assembly Handling and Baking Requirements

After opening the sealed tape-and-reel, components should be used within 168 hours.

- For standard packages: If the 168-hour limit is exceeded, bake at 125 ℃ for 2 hours before use.
- For vacuum tape-and-reel QFN packages: The tape material is not heat-resistant. If baking is required (i.e., after 168 hours), it must be performed at 85 ℃ for 360 hours. This special condition supersedes the standard baking procedure.

Note: Proper baking is critical to remove moisture and prevent damage during the subsequent reflow soldering process.